AN947: Implementing Zero Delay Mode Using the Si5340/41/42/44/45/80

A zero delay clock generator or buffer is one whose outputs are edge-aligned with a reference clock. This should not be confused with phase-lock, as phase-lock refers to two clocks that are on average aligned in phase with some (often unknown) initial phase offset. A zero delay clock, on the other hand, has no or minimal initial phase offset.

Applications of the Si5340/41/42/44/45/80 zero delay feature exist in many synchronous systems, such as SONET/SDH networks, synchronous Ethernet, PCIe and other high-speed interconnects, and any application requiring known and predictable delay between a reference and one or more output clocks.

KEY FEATURES

- Zero delay removes (minimizes) input-to-output propagation delays to produce outputs phase-aligned to the input clocks for applications requiring minimal, known, and/or predictable delays
- Supported on Si5340/41/42/44/45 and Si5380
- Easy to set up using ClockBuilder Pro

1. Introduction

In a typical clock generator or jitter attentuator there is usually some propagation delay from the input reference clock to the outputs. This delay can have uncertainty due to frequency plan differences, variations across process and temperature, and variations between subsequent device resets. Using the zero delay feature available in the Si5340/41/42/44/45/80 family of clock generators and jitter attenuators we can zero out any input-to-output propagation delay and minimize uncertainty.

This application note provides details on setting up a zero delay frequency plan and testing it on an evaluation board. A ClockBuilder Pro example is shown using the Si5345; however, other devices can also be set up similarly.

2. Theory of Operation

The figure below shows a high-level block diagram of the Si5342/44/45 devices. The PLL works to zero out steady-state phase error between the two inputs of its phase detector (PD), a reference clock input and a feedback input. This is not very useful in terms of input-to-output edge alignment; any edge alignment information is lost due to the fixed and variable delays in the feedback M divider, output Multisynth and R dividers, and the input P divider.

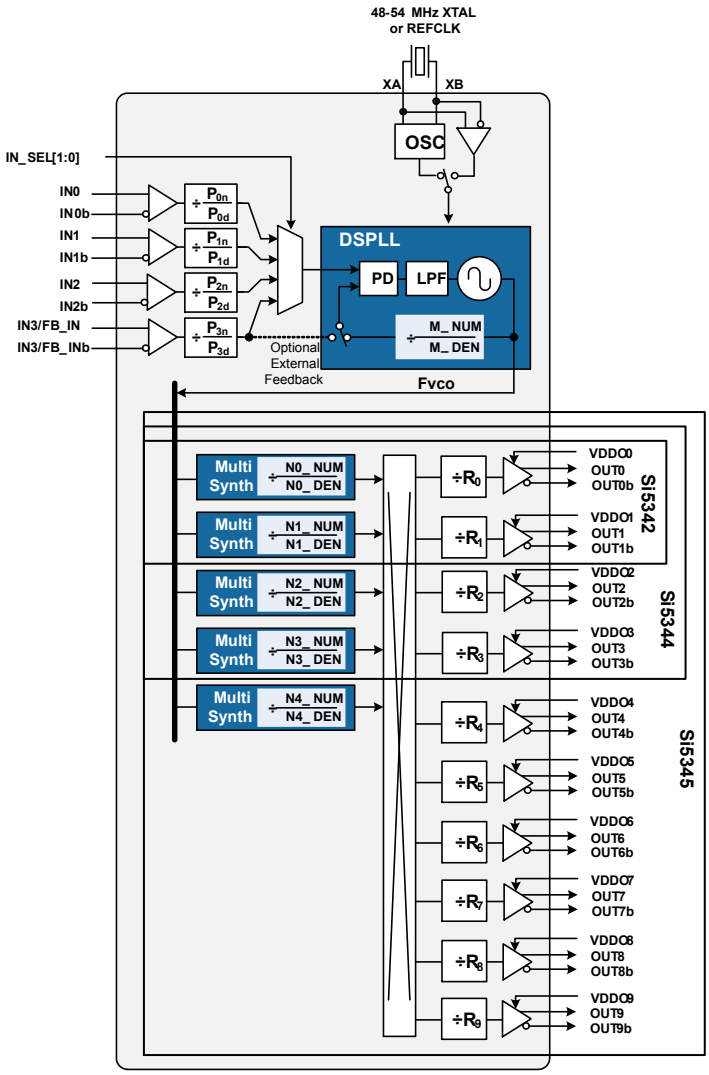

Figure 2.1. Si5342/44/45 in Standard PLL Mode

If we replace the feedback input of the PD with one of the output clocks, as shown in the figure below, we can edge align all related outputs with the input clocks. Note that edge alignment occurs at the PD input. Care was taken in the design of the Si534x/8x family to match propagation delays between multiple input paths and output dividers. This allows multiple outputs to be zero delay with respect to any one of the inputs.

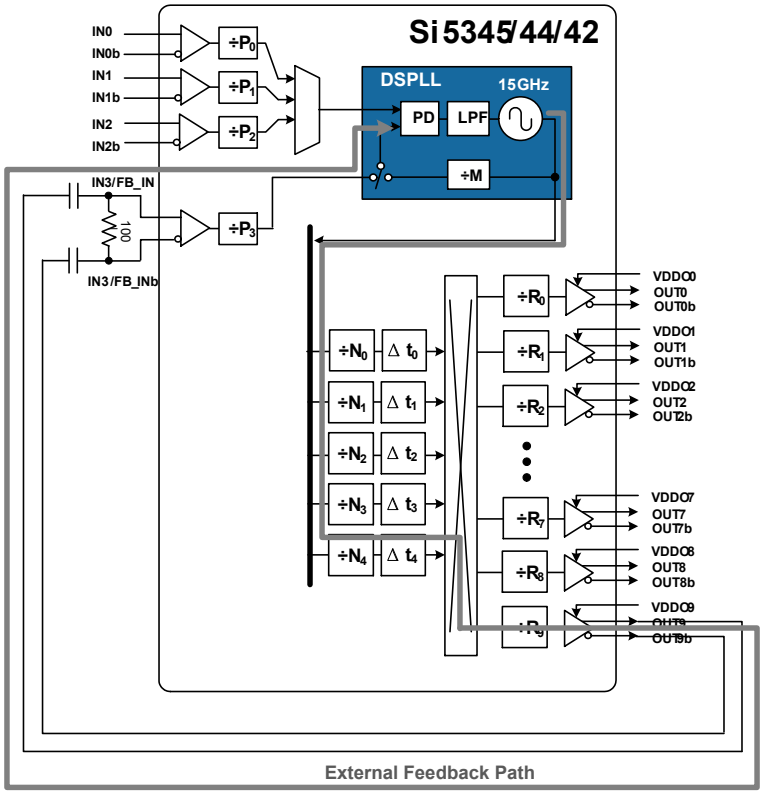

Figure 2.2. Si5345 Zero Delay Mode Set-up

3. Setup

Any of the Si5340/41/42*/44*/45/80 devices can be configured for zero delay mode using Clock Builder Pro. The output closest to the IN3/FBIN pins (OUT2, OUT3, or OUT9 depending on the device variant) must be tied to IN3/FBIN. Care must be taken in layout to minimize trace length and any exposure to noise sources on the PCB.
Note: Zero delay mode is not available on the Si5342H/44H.

3.1 Setting up zero delay mode using ClockBuilder Pro

In the Zero Delay Mode tab of the ClockBuilder Pro wizard check *Enable Zero Delay Mode.* Leave external feedback output selection to its default value.

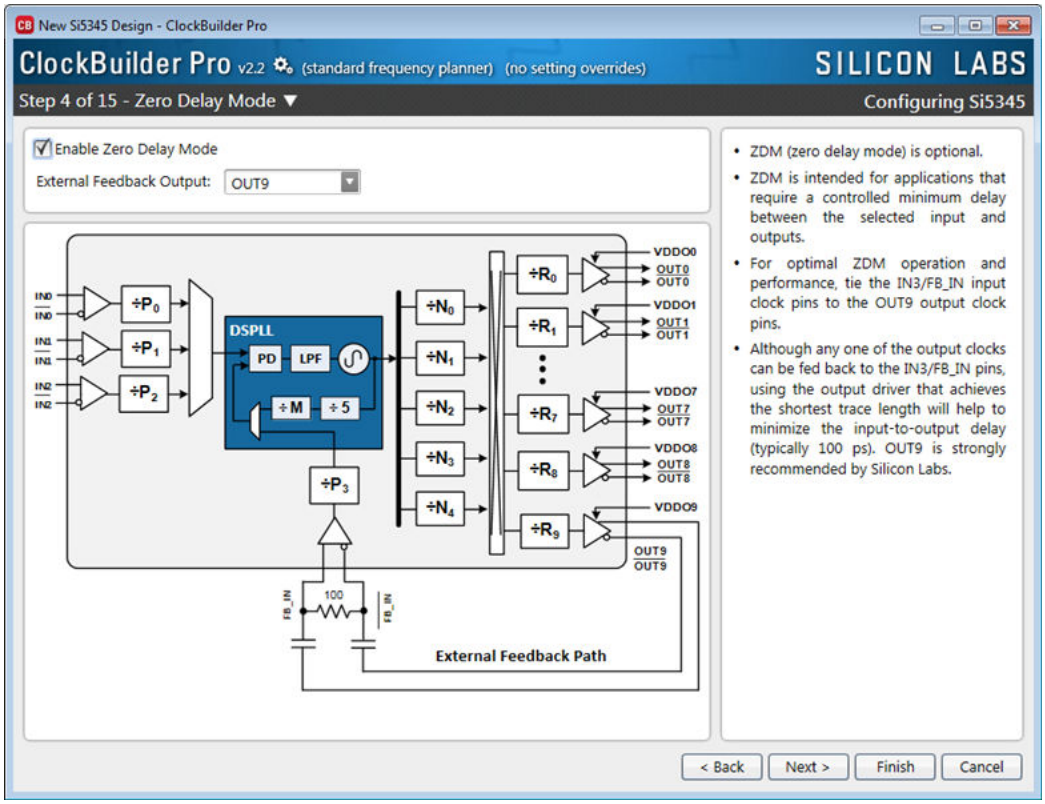

Figure 3.1. ClockBuilder Pro Wizard--Zero Delay Step

This will block out IN3 as an input clock. Note that automatic input clock switching is not available if there are multiple input clocks and zero delay mode is enabled. One of the manual input clock selections must be used, registers or pins (see the figure below).

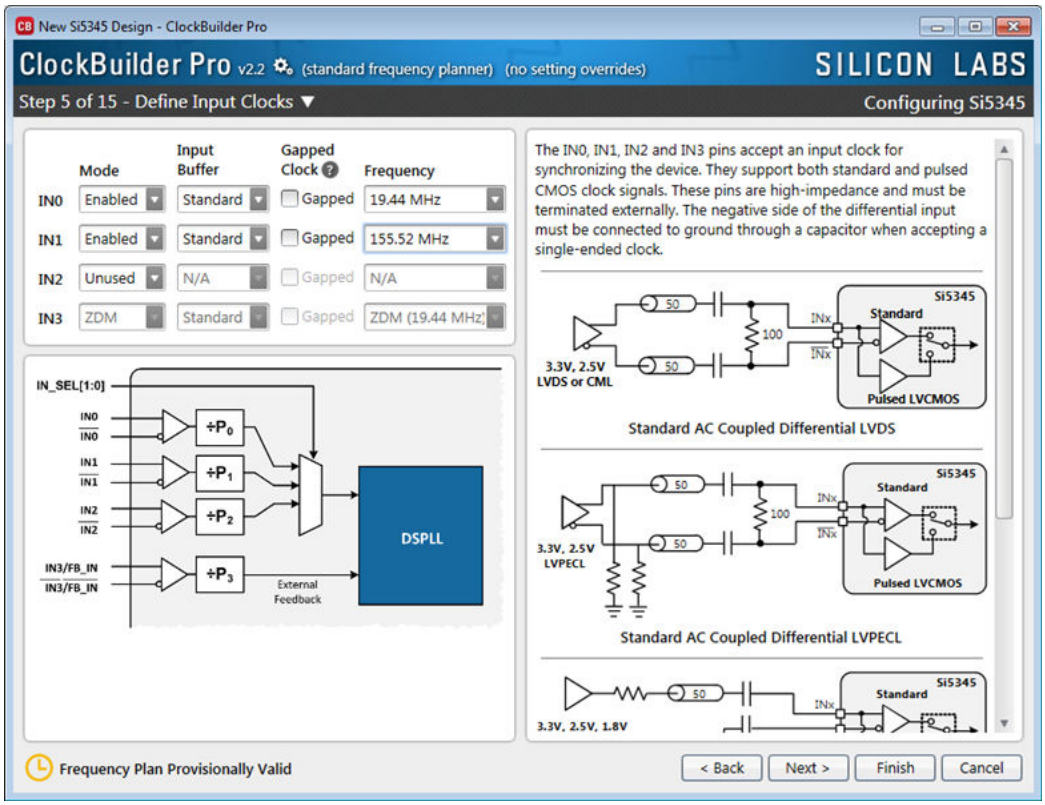

Figure 3.2. ClockBuilder Pro Wizard--Define Input Clocks Step

In the Define Output Frequencies Step, the Clockbuilder Pro frequency planning algorithm will attempt to derive all related frequencies from the N0/ZDM Multisynth divider. This will ensure edge alignment for integer-related frequencies such as 19.44 MHz and 155.52 MHz as shown in the figure below. Zero-delayed outputs can also be explicitly selected by using the N divider/DCO/ZDM pull-down selection.

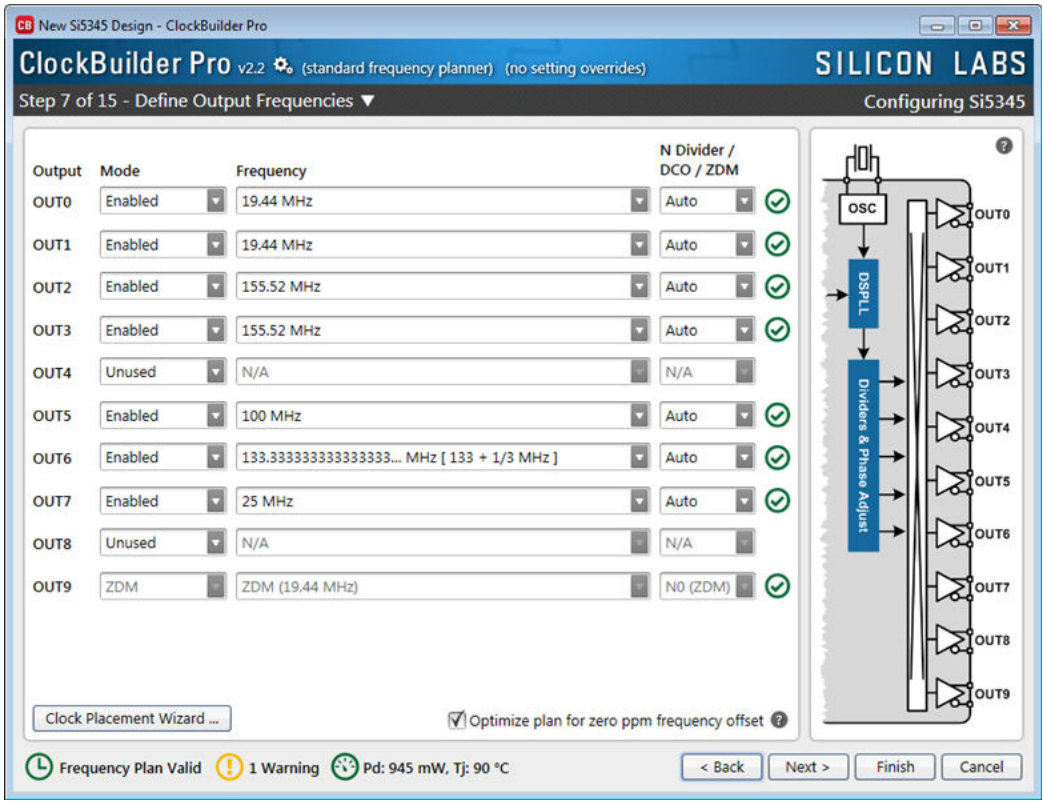

Figure 3.3. ClockBuilder Pro Wizard--Define Output Frequencies Step

3.2 Zero Delay Mode Registers

3.2.1 Si5340/41 Zero Delay Mode Registers

Table 3.1. Si5340/41 Zero Delay Mode Registers

Reg Address	Bit Field	Type	Setting Name	Description
0x091C	2:0	R/W	ZDM_EN	3=Zero delay mode 4=Normal mode All other values must not be written.
0x0021	0	R/W	IN_SEL_REGCTRL	0: pin controlled clock selection 1: register controlled clock selection
0x0140[3:0]	3:0	R/W	OUTX_ALWAYS_ON	0x100: Si5340 (OUT3) 0x800: Si5341 (OUT9) Output tied to IN3/FBIN must be configured to always on.
0x0139[3:0]	7:0			

3.2.2 Si5342/44/45/80 Zero Delay Mode Registers

Table 3.2. Si5342/44/45/80 Zero Delay Mode Registers

Reg Address	Bit Field	Type	Setting Name	Description
0x0140 0x0139	3:0 7:0	R/W	OUTX_ALWAYS_ON	0x10: Si5342 (OUT2) 0x100: Si5344 (OUT3) 0x800: Si3545/80 Output tied to IN3/FBIN must be configured to always on.
0x0487	0	R/W	ZDM_EN	0: Disable zero delay mode. 1: Enable zero delay mode.
0x0487	2:1	R/W	ZDM_IN_SEL	When zero delay is enabled, this register parameter selects the input clock in manual register controlled mode. Ignore if device set up in pin controlled mode. 0: IN0 1: IN1 2: IN2 3: A register value of 3 is not allowed.
0x052A	0	R/W	IN_SEL_REGCTRL	0: pin controlled clock 1: register controlled clock selection

When ZDM_EN is high the IN_SEL register bits become unused. Instead ZDM_IN_SEL register bits must be used. If ZDM_EN and IN_SEL_REGCTRL are both high, clock selection is pin-controlled and neither IN_SEL or ZDM_IN_SEL are used.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
www.silabs.com/timing

SW/HW
www.silabs.com/CBPro

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com