4-Output Low Jitter Any-Frequency Clock Generator

```
Overview
========
Part:          Si5340
Design ID:     5340BP2
Created By:    ClockBuilder Pro v1.7 [2015-03-26]
Timestamp:     2015-03-26 09:25:10 GMT-05:00

Device Grade
============

Device     Output Clock          Supported Frequency Synthesis Modes
Grade      Frequency Range       (Typical Jitter)
---------  -----------------     ----------------------------------------
Si5340A    100 Hz to 712.5 MHz   Integer (<100 fs) and fractional (< 150 fs)
Si5340B    100 Hz to 350 MHz     "
Si5340C    100 Hz to 712.5 MHz   Integer only (< 100 fs)
Si5340D*   100 Hz to 350 MHz     "

* Device Grade

Design
======
Host Interface:
   I/O Power Supply: VDD (Core)
   SPI Mode: 4-Wire
   I2C Address Range: 116d to 119d / 0x74 to 0x77 (selected via A0/A1 pins)

Inputs:
   XAXB: Unused
    IN0: Unused
    IN1: Unused
    IN2: Unused

Outputs:
   OUT0: Unused
   OUT1: Unused
   OUT2: Unused
   OUT3: Unused

Frequency Plan
==============
No plan

Settings
========

Location      Setting Name          Decimal Value  Hex Value
------------  --------------------  -------------  --------------
0x000B[0:6]   I2C_ADDR              116            0x74
0x0017[0]     SYSINCAL_INTR_MSK     0              0x0
0x0017[1]     LOSXAXB_INTR_MSK      0              0x0
0x0017[2]     LOSREF_INTR_MSK       0              0x0
0x0017[3]     LOL_INTR_MSK          0              0x0
0x0017[5]     SMB_TMOUT_INTR_MSK    0              0x0
0x0018[0:3]   LOSIN_INTR_MSK        15             0xF
0x0021[0]     IN_SEL_REGCTRL        0              0x0
0x0021[1:2]   IN_SEL                0              0x0
0x0022[1]     OE                    0              0x0
0x002B[3]     SPI_3WIRE             0              0x0
0x002B[5]     AUTO_NDIV_UPDATE      0              0x0
```

0x002C[0:3]	LOS_EN	0	0x0
0x002C[4]	LOSXAXB_DIS	1	0x1
0x002D[0:1]	LOS0_VAL_TIME	0	0x0
0x002D[2:3]	LOS1_VAL_TIME	0	0x0
0x002D[4:5]	LOS2_VAL_TIME	0	0x0
0x002D[6:7]	LOS3_VAL_TIME	0	0x0
0x002E[0:15]	LOS0_TRG_THR	0	0x0000
0x0030[0:15]	LOS1_TRG_THR	0	0x0000
0x0032[0:15]	LOS2_TRG_THR	0	0x0000
0x0034[0:15]	LOS3_TRG_THR	0	0x0000
0x0036[0:15]	LOS0_CLR_THR	0	0x0000
0x0038[0:15]	LOS1_CLR_THR	0	0x0000
0x003A[0:15]	LOS2_CLR_THR	0	0x0000
0x003C[0:15]	LOS3_CLR_THR	0	0x0000
0x0041[0:4]	LOS0_DIV_SEL	0	0x00
0x0042[0:4]	LOS1_DIV_SEL	0	0x00
0x0043[0:4]	LOS2_DIV_SEL	0	0x00
0x0044[0:4]	LOS3_DIV_SEL	0	0x00
0x009E[4:7]	LOL_SET_THR	0	0x0
0x0102[0]	OUTALL_DISABLE_LOW	1	0x1
0x0112[0]	OUT0_PDN	1	0x1
0x0112[1]	OUT0_OE	0	0x0
0x0112[2]	OUT0_RDIV_FORCE2	0	0x0
0x0113[0:2]	OUT0_FORMAT	1	0x1
0x0113[3]	OUT0_SYNC_EN	1	0x1
0x0113[4:5]	OUT0_DIS_STATE	0	0x0
0x0113[6:7]	OUT0_CMOS_DRV	0	0x0
0x0114[0:3]	OUT0_CM	11	0xB
0x0114[4:6]	OUT0_AMPL	3	0x3
0x0115[0:2]	OUT0_MUX_SEL	0	0x0
0x0115[6:7]	OUT0_INV	0	0x0
0x0117[0]	OUT1_PDN	1	0x1
0x0117[1]	OUT1_OE	0	0x0
0x0117[2]	OUT1_RDIV_FORCE2	0	0x0
0x0118[0:2]	OUT1_FORMAT	1	0x1
0x0118[3]	OUT1_SYNC_EN	1	0x1
0x0118[4:5]	OUT1_DIS_STATE	0	0x0
0x0118[6:7]	OUT1_CMOS_DRV	0	0x0
0x0119[0:3]	OUT1_CM	11	0xB
0x0119[4:6]	OUT1_AMPL	3	0x3
0x011A[0:2]	OUT1_MUX_SEL	0	0x0
0x011A[6:7]	OUT1_INV	0	0x0
0x0126[0]	OUT2_PDN	1	0x1
0x0126[1]	OUT2_OE	0	0x0
0x0126[2]	OUT2_RDIV_FORCE2	0	0x0
0x0127[0:2]	OUT2_FORMAT	1	0x1
0x0127[3]	OUT2_SYNC_EN	1	0x1
0x0127[4:5]	OUT2_DIS_STATE	0	0x0
0x0127[6:7]	OUT2_CMOS_DRV	0	0x0
0x0128[0:3]	OUT2_CM	11	0xB
0x0128[4:6]	OUT2_AMPL	3	0x3
0x0129[0:2]	OUT2_MUX_SEL	0	0x0
0x0129[6:7]	OUT2_INV	0	0x0
0x012B[0]	OUT3_PDN	1	0x1
0x012B[1]	OUT3_OE	0	0x0
0x012B[2]	OUT3_RDIV_FORCE2	0	0x0
0x012C[0:2]	OUT3_FORMAT	1	0x1
0x012C[3]	OUT3_SYNC_EN	1	0x1
0x012C[4:5]	OUT3_DIS_STATE	0	0x0
0x012C[6:7]	OUT3_CMOS_DRV	0	0x0
0x012D[0:3]	OUT3_CM	11	0xB
0x012D[4:6]	OUT3_AMPL	3	0x3
0x012E[0:2]	OUT3_MUX_SEL	0	0x0
0x012E[6:7]	OUT3_INV	0	0x0

0x013F[0:11]	OUTX_ALWAYS_ON	0	0x000
0x0141[5]	OUT_DIS_LOL_MSK	0	0x0
0x0141[7]	OUT_DIS_MSK_LOS_PFD	0	0x0
0x0202[0:31]	XAXB_FREQ_OFFSET	0	0x00000000
0x0206[0:1]	PXAXB	0	0x0
0x0208[0:47]	P0	0	0x000000000000
0x020E[0:31]	P0_SET	0	0x00000000
0x0212[0:47]	P1	0	0x000000000000
0x0218[0:31]	P1_SET	0	0x00000000
0x021C[0:47]	P2	0	0x000000000000
0x0222[0:31]	P2_SET	0	0x00000000
0x0226[0:47]	P3	0	0x000000000000
0x022C[0:31]	P3_SET	0	0x00000000
0x0235[0:43]	M_NUM	0	0x00000000000
0x023B[0:31]	M_DEN	0	0x00000000
0x0250[0:23]	R0_REG	0	0x000000
0x0253[0:23]	R1_REG	0	0x000000
0x025C[0:23]	R2_REG	0	0x000000
0x025F[0:23]	R3_REG	0	0x000000
0x026B[0:7]	DESIGN_ID0	53	0x35
0x026C[0:7]	DESIGN_ID1	51	0x33
0x026D[0:7]	DESIGN_ID2	52	0x34
0x026E[0:7]	DESIGN_ID3	48	0x30
0x026F[0:7]	DESIGN_ID4	66	0x42
0x0270[0:7]	DESIGN_ID5	80	0x50
0x0271[0:7]	DESIGN_ID6	50	0x32
0x0272[0:7]	DESIGN_ID7	0	0x00
0x0302[0:43]	N0_NUM	0	0x00000000000
0x0308[0:31]	N0_DEN	0	0x00000000
0x030D[0:43]	N1_NUM	0	0x00000000000
0x0313[0:31]	N1_DEN	0	0x00000000
0x0318[0:43]	N2_NUM	0	0x00000000000
0x031E[0:31]	N2_DEN	0	0x00000000
0x0323[0:43]	N3_NUM	0	0x00000000000
0x0329[0:31]	N3_DEN	0	0x00000000
0x0339[0:4]	N_FSTEP_MSK	31	0x1F
0x033B[0:43]	N0_FSTEPW	0	0x00000000000
0x0341[0:43]	N1_FSTEPW	0	0x00000000000
0x0347[0:43]	N2_FSTEPW	0	0x00000000000
0x034D[0:43]	N3_FSTEPW	0	0x00000000000
0x0359[0:15]	N0_DELAY	0	0x0000
0x035B[0:15]	N1_DELAY	0	0x0000
0x035D[0:15]	N2_DELAY	0	0x0000
0x035F[0:15]	N3_DELAY	0	0x0000
0x090E[0]	XAXB_EXTCLK_EN	0	0x0
0x090E[1]	XAXB_PDNB	0	0x0
0x091C[0:2]	ZDM_EN	4	0x4
0x0943[0]	IO_VDD_SEL	0	0x0
0x0949[0:3]	IN_EN	8	0x8
0x0949[4:7]	IN_PULSED_CMOS_EN	0	0x0
0x0A02[0:4]	N_ADD_0P5	0	0x00
0x0A03[0:4]	N_CLK_TO_OUTX_EN	15	0x0F
0x0A04[0:4]	N_PIBYP	0	0x00
0x0A05[0:4]	N_PDNB	15	0x0F
0x0B44[0:3]	PDIV_ENB	0	0x0
0x0B4A[0:4]	N_CLK_DIS	0	0x00

This datasheet addendum is provided as supplemental information to the Si5340D datasheet, located at www.silabs.com/timing. You can search for and download any datasheet addendum for Si534x/8x part numbers. Go to http://www.silabs.com/custom-timing for more information.

Silicon Laboratories

400 West Cesar Chavez
Austin, TX 78701
Phone (512) 416-8500
www.silabs.com