ClockBuilder Pro Applications Notice: Si534x Parts-Per-Trillion Frequency Offset

A frequency offset issue in a small percentage of Si534x devices' frequency plans can result in an offset between <1 and 10,000 parts-per-trillion (ppt). This frequency offset issue can affect any of the following base ordering part numbers (OPNs), or custom ordering part numbers:

- Si5342
- Si5344
- Si5345
- Si5346
- Si5347

This Applications Notice describes the frequency offset issue and how to use CBPro v2.0 or later to update a frequency plan to eliminate the offsets.

KEY POINTS

- Downloads and use ClockBuilder Pro v2.0 or later to develop or update frequency plans which do not exhibit the parts-per-trillion frequency offset issue
- Refer to the Product Bulletin for more information
- Contact Silicon Labs Technical Support if you need more information or help with your frequency plan

1. Introduction

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- Si5344
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- Si5346
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This Applications Notice describes the frequency offset issue and how to use CBPro to update a frequency plan to eliminate the offsets.

2. Parts-per-trillion Frequency Offset Description

Referring to Figures 1-5, in some frequency plans, where either the Px or Mx values are not integers, a small output frequency offset is created. The total offset is always less than 10,000 ppt, and typically less than 1 ppt. This offset is caused by an underlying issue in the device's design of how it manipulates the fractional part of the quotient. Frequency offsets of this small magnitude are difficult to measure and in many systems will not cause any deleterious behavior.

Internally, the quotient is represented as an integer portion plus a numerator and a denominator and a remainder. The numerator and denominators are represented by 32-bit registers, with both left shifted as much as possible to maximize the representation. Due to processing errors, the last bit can be incorrectly modulated, resulting in a very small error. This processing error is in the Px and Mx dividers and is active only when they are not integers.

If the M divider is used[1] for the finc/fdec feature of the device to adjust the output frequency, the M divider is likely to use a value that triggers this frequency offset issue. Since using finc/fdec causes the M values to change, there is no single frequency plan that will prevent this from happening. Generally, applications that use finc/fdec are adjusting the frequency to match an external clock and the offset caused by this error will be unnoticeable since the finc/fdec adjustments are orders of magnitude greater than the offset caused by the error.

[1] The M divider is commonly used in the Si5346/Si5347 for finc/fdec.

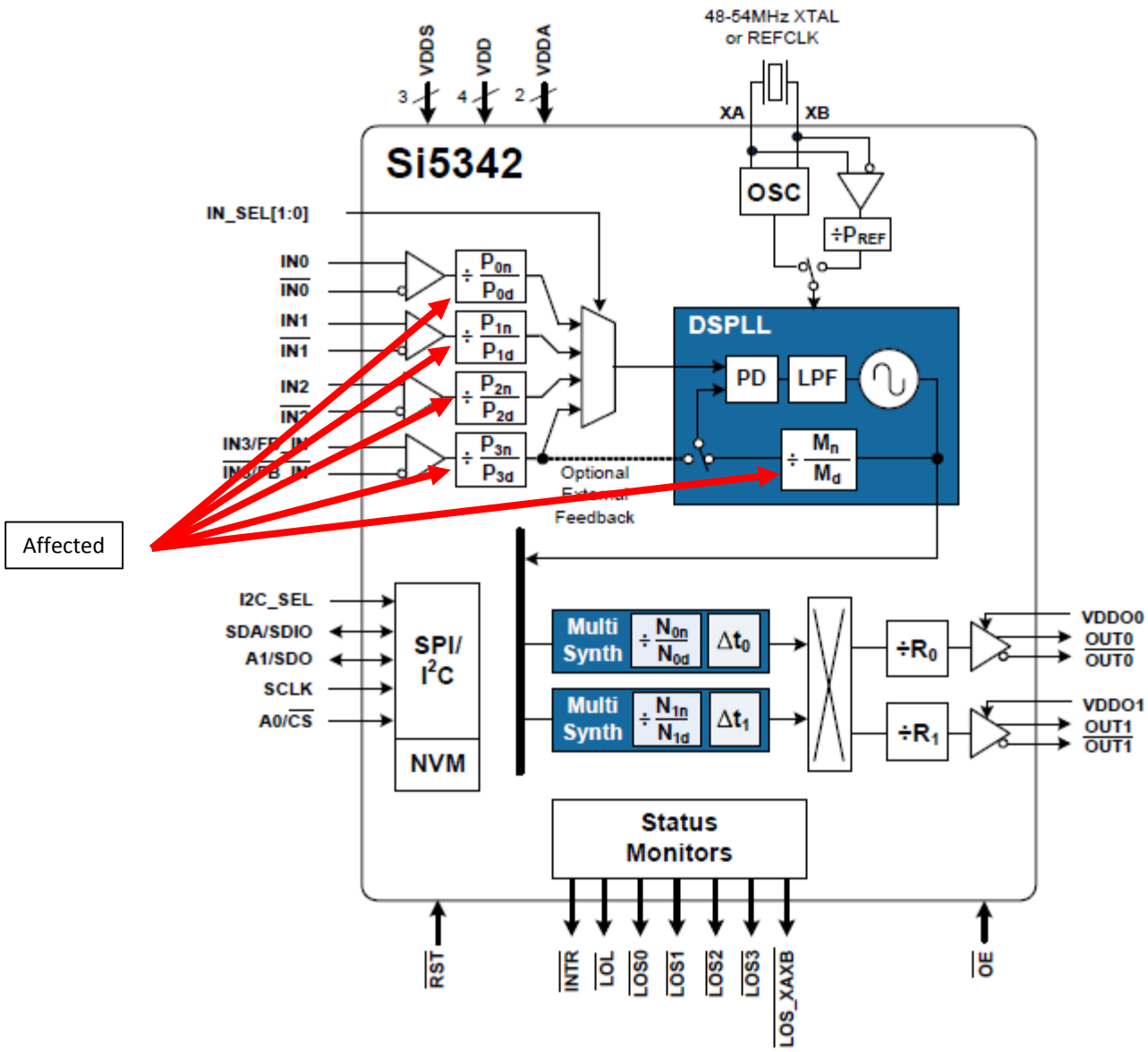


Figure 1 – Si5344 Affected Dividers

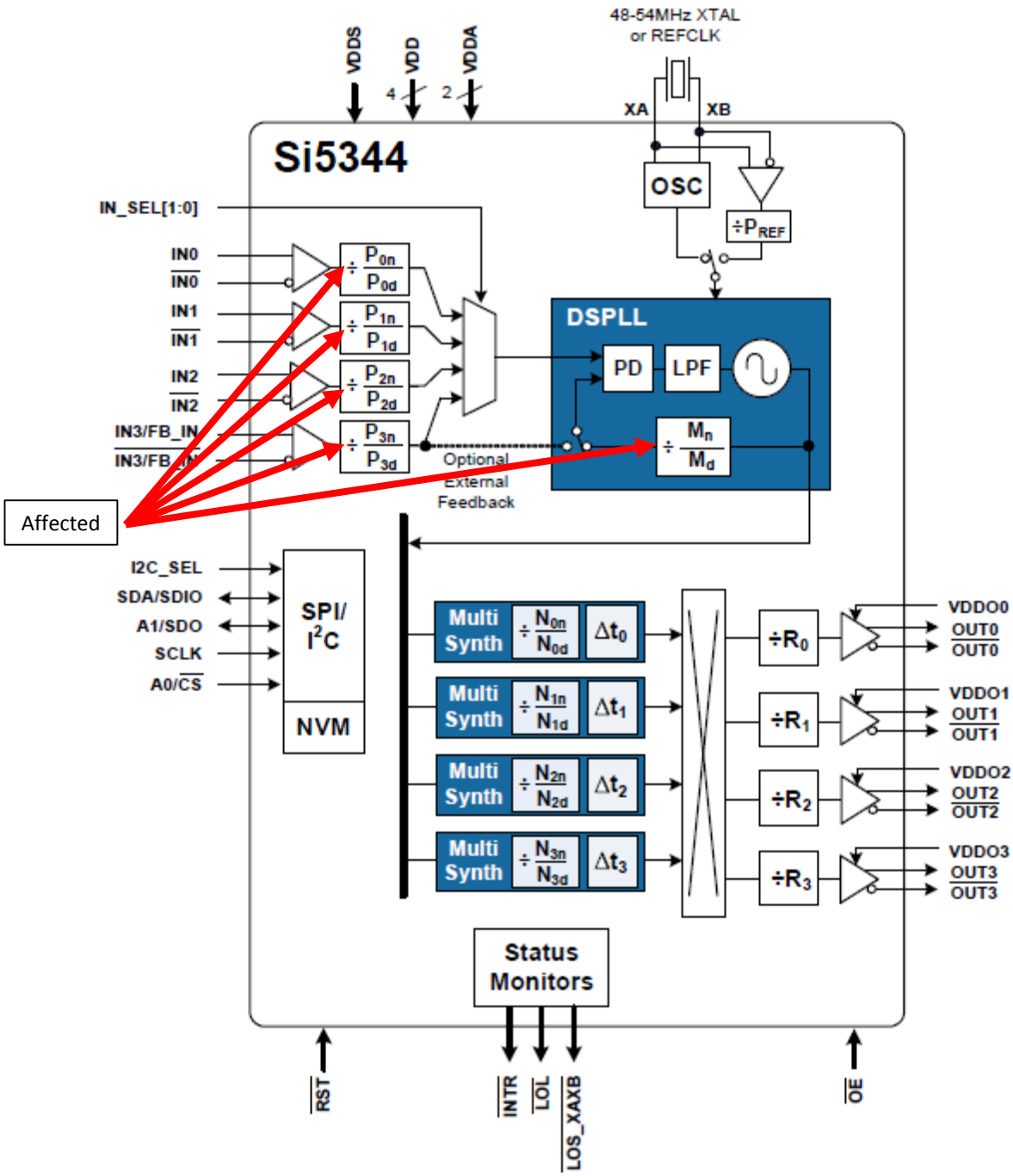


Figure 2 – Si5344 Affected Dividers

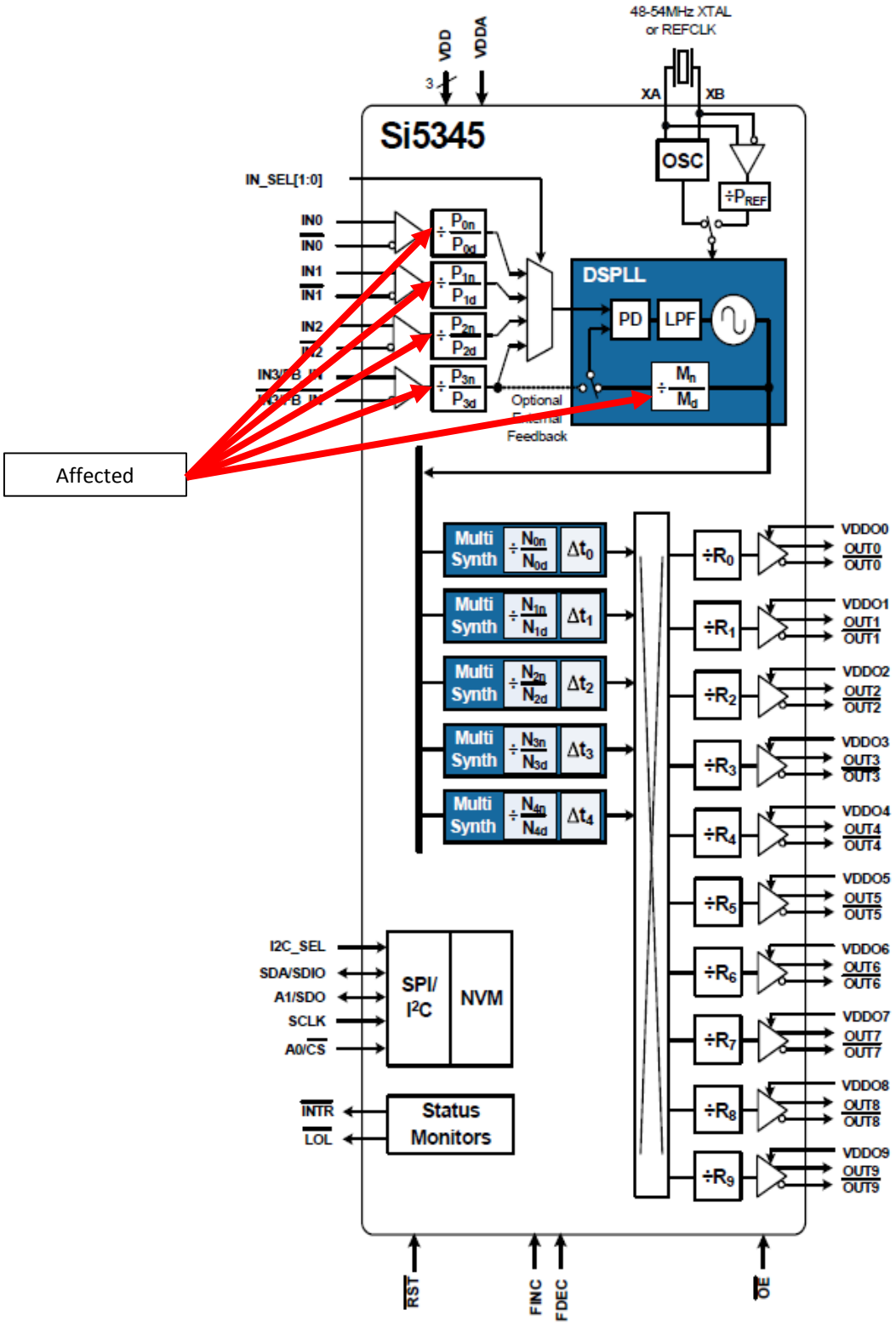


Figure 3 – Si5345 Affected Dividers

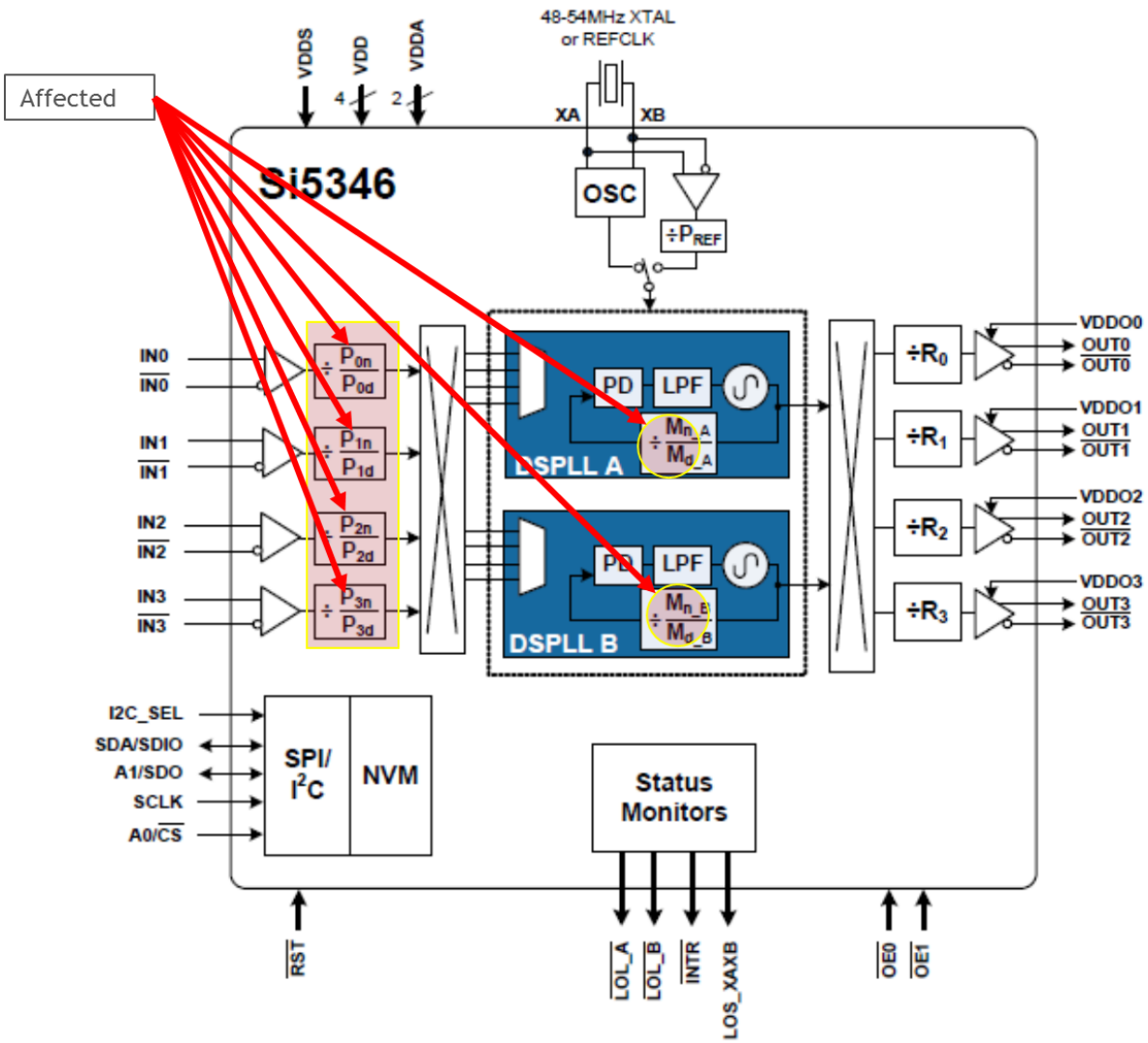


Figure 4 – Si5346 Affected Dividers

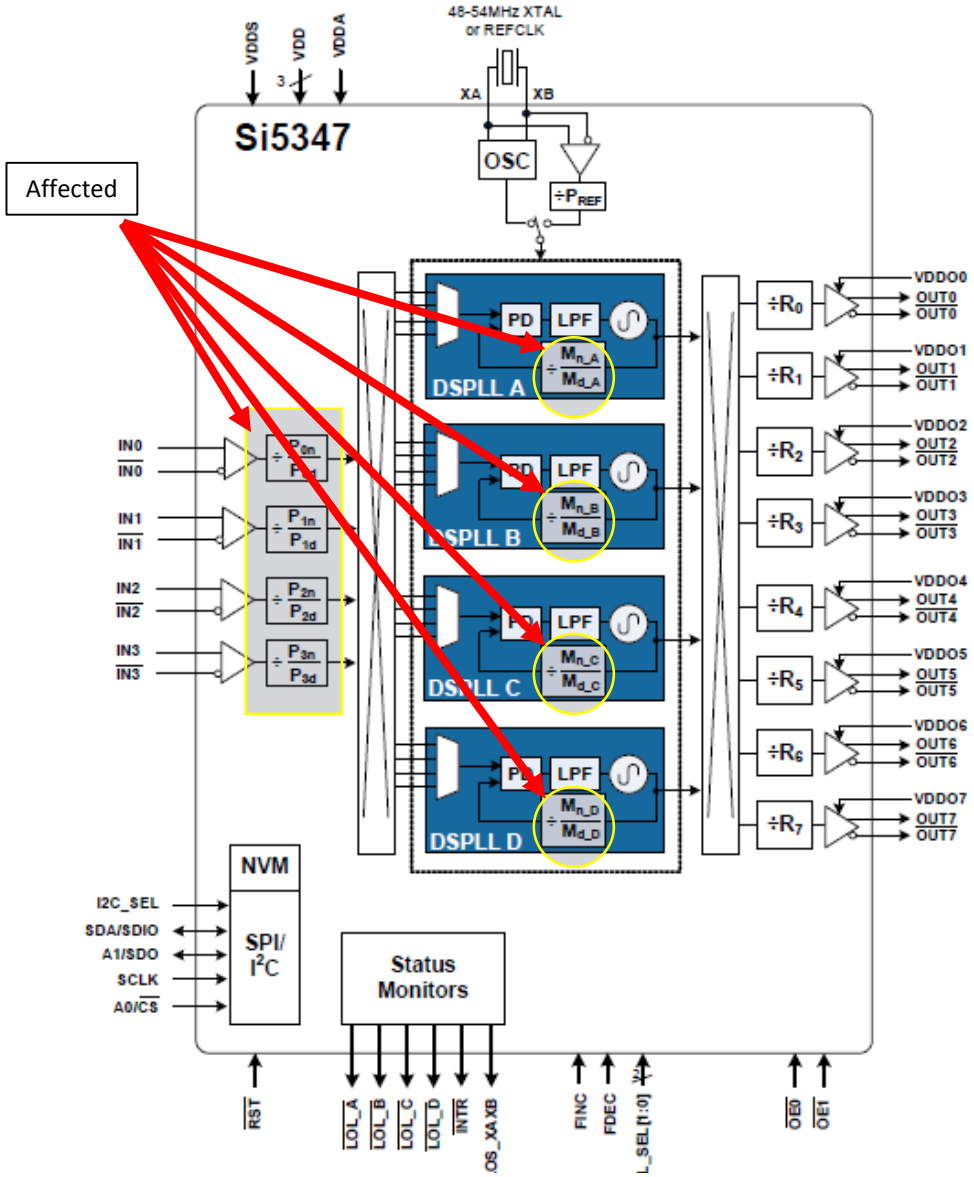


Figure 5 – Si5347 Affected Dividers

3. Workarounds

Recent CBPro enhancements address this frequency offset issue. Please download version 1.9 or later. Users are strongly advised to update all copies of CBPro to the latest version. Earlier versions of CBPro do not address this issue and using earlier versions may result in a plan that has a frequency offset. Always open a CBPro project file with the version that created it or later.

After opening an existing project file, CBPro will analyze the frequency plan for this frequency offset issue and re-calculate the entire frequency plan to use the latest CBPro algorithms. There are three possible outcomes at this point (See Figure 7 for the suggested workflow for using CBPro to address this is issue).

3.1 No Problem Found

No problem found and the frequency plan is up to date: CBPro opens as usual. There is no special notification.

3.2 Frequency Offset Problem Found, but the frequency plan needs to be updated

No problem found (Figure X), but the analyzed plan was created by an earlier version of CBPro and needs to be updated with the latest algorithms from CBPro.

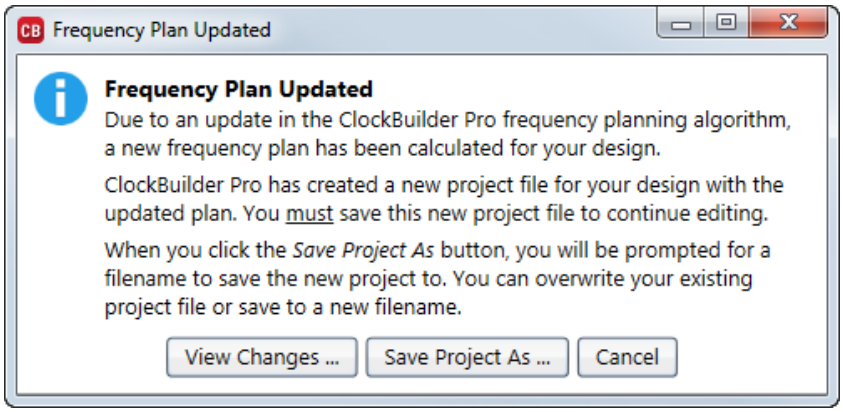


Figure 6 – Frequency Plan Update is Required, Plan Does Not Exhibit Offset Issue

3.3 There is a frequency offset problem with this plan

The project file is affected by the frequency offset issue (See **Error! Reference source not found.**). This dialog has a few new buttons for users.

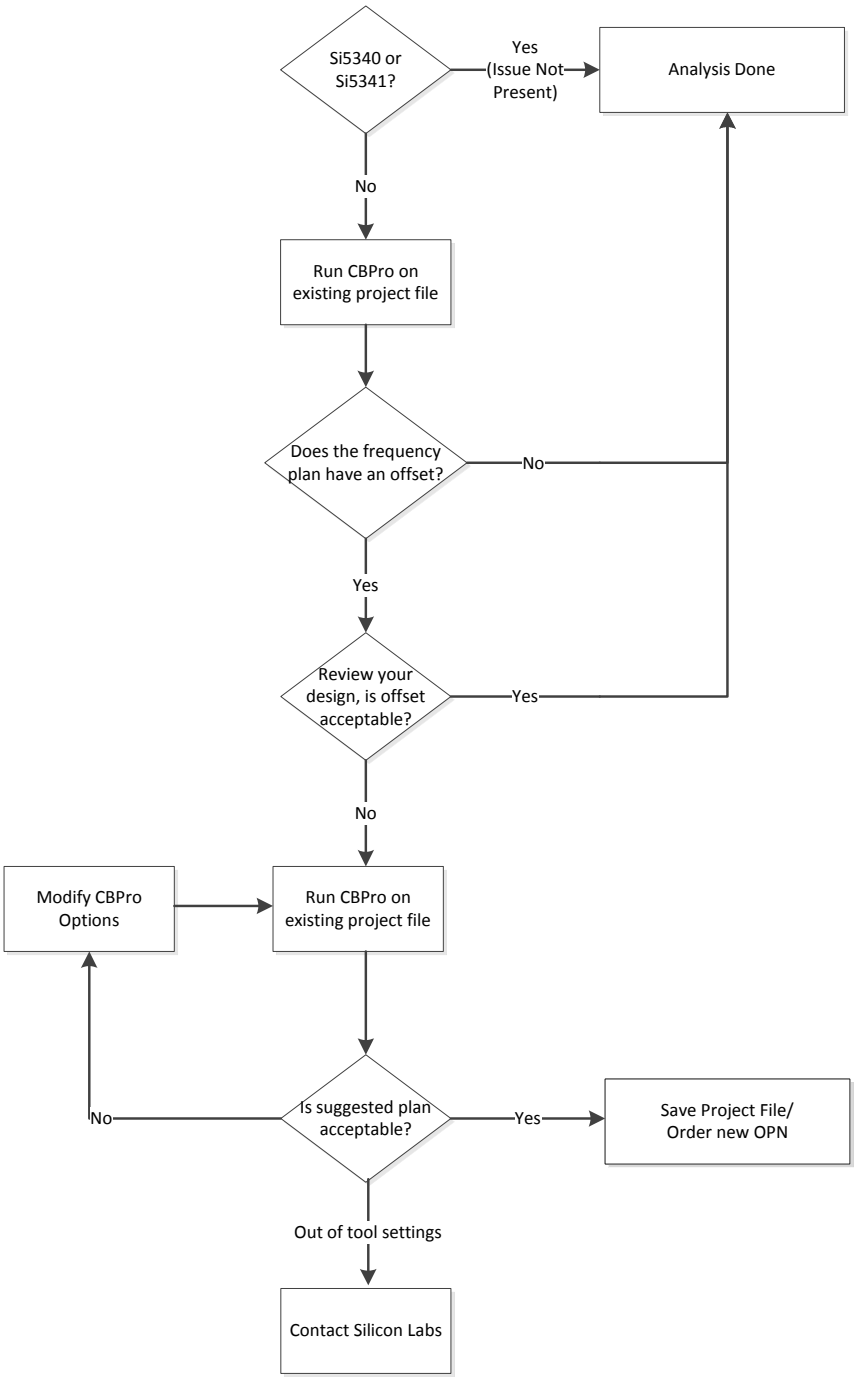


Figure 7 – User Steps to Investigating Frequency Offset Issue

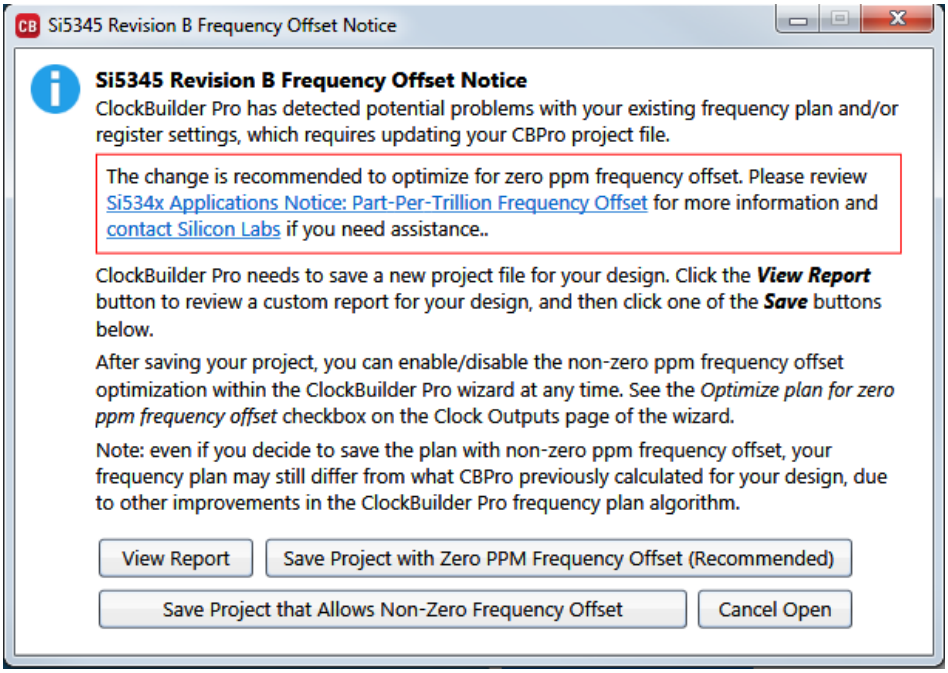


Figure 8 - Existing Frequency Plan Exhibits the Offset Issue

3.3.1 View Report

Provides a before and after comparison of the frequency plans, including the estimated maximum frequency offset (typically, the offset is much less than the listed maximum). The report shows three plans:

- ***CBPro vx.x Plan+Settings:*** The first is the current plan that has the frequency offset problem. The other two columns will show in yellow any variations from the current plan. Included in this column is the maximum offset on an output-by-output basis.
- ***CBPro vx.x Plan+Settings, Allow Non-Zero PPM Offset:*** CBPro provides an option to use its updated algorithms and allow frequency offset solutions. This is not the recommended plan, but there are applications that can tolerate the offset. This plan will generally be closer to the original frequency plan.
- ***CBPro vx.x Plan+Settings, Require Zero PPM Offset (Recommended):*** This frequency plan has no frequency offset. In general, this is the preferred plan, since it eliminates the offset. Inspect the plan for its suitability in terms of the other changes made by CBPro, such as bandwidth and meeting the frequency requirements for hitless switching.

Review the results for any impact on your application and select which plan best fits your needs. If you elect to keep the current plan, you must hit “Cancel Open.” It is not possible to continue using CBPro on this plan without selecting one of the other plans.

3.3.2 Save Project that allows Non-Zero Frequency Offset

Updates the project file with frequency offsets per the column labeled “CBPro vx.x Plan+Settings, Allow Non-Zero PPM Offset.” After saving the project, the CBPro program is opened and changes can be made.

3.3.3 Save Project with Zero PPM Frequency Offset (Recommended)

Updates the project file to eliminate all offsets per the column labeled “CB CBPro vx.x Plan+Settings, Require Zero PPM Offset (Recommended).” After saving the project, the CBPro program is opened and changes can be made.

4. Impacts without Workarounds

On those outputs that CBPro identifies as being affected, the nominal output frequency is very slightly off. Using the Si5345 as an example, Equation 1 and **Figure 9** illustrate the expected frequency relationship between the inputs and outputs and a simplified signal flow through the part. Note that the dividers M and N are internally represented as a numerator over a denominator (Mn/Md or Pn/Pd).

$$F_{out} = F_{in} * \frac{M}{P*N*R} \qquad \textbf{Equation 1}$$

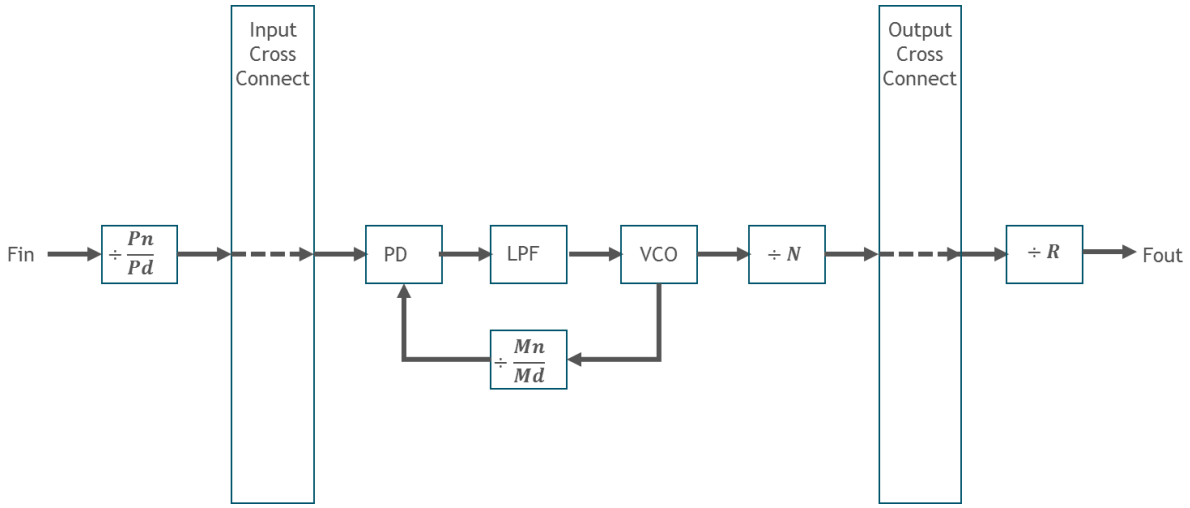


Figure 9 – Si5345 PLL Block Diagram

In cases where M or P are ***not*** integers, there is a design error in how the device processes fractional M and P values. Use CBPro to calculate the maximum value of this offset in your frequency plan. If the settings of the device and the frequency plan are not changed, this offset will always be present. In many systems, this offset is acceptable.

Figure 10 illustrates the time required to observe a full period slip, depending on the clock frequency and the offset. In many systems, FIFOs are typically in the data path and the time to observe a FIFO overflow/underflow will take considerably longer. Every application is different: in some systems offsets of this magnitude will have no negative effect; and in other systems it may cause data corruption. You will need to examine the requirements of your system in light of very small frequency offsets in the output of the device. If the offsets are acceptable, no further action is required.

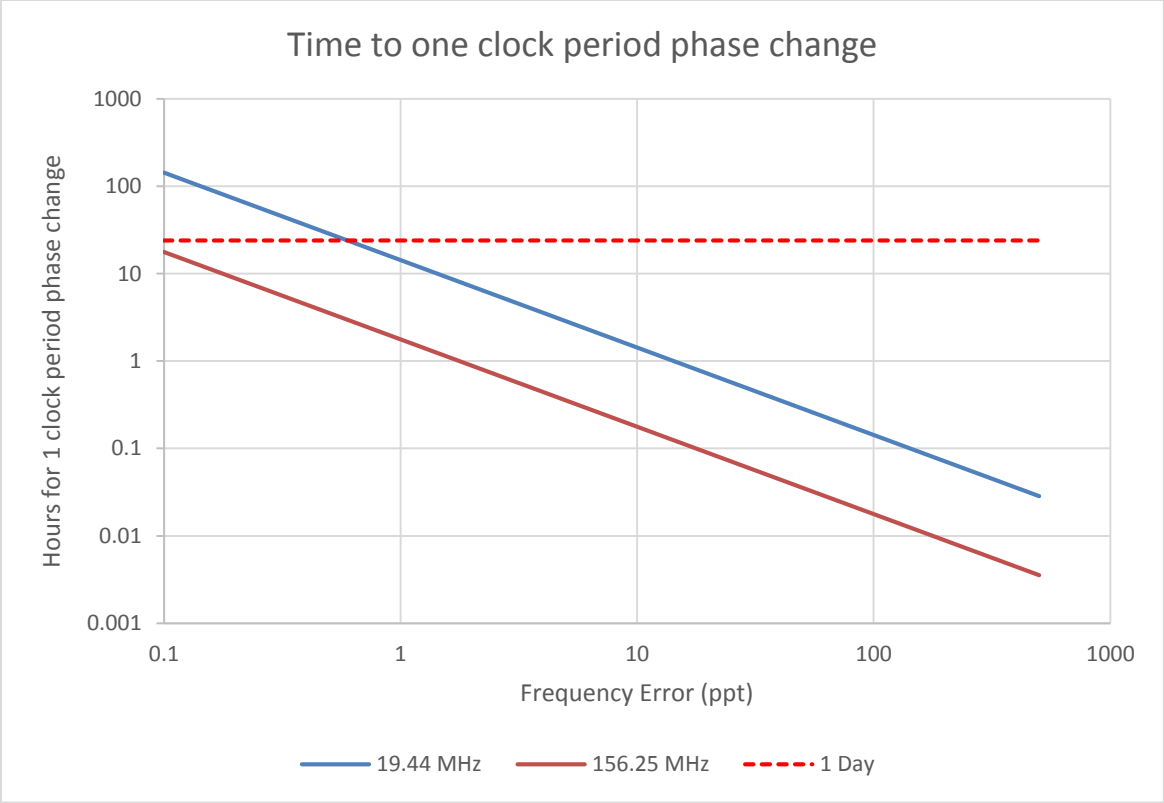


Figure 10 – Time to one clock period slip vs frequency offset

5. Using CBPro to Calculate a New Project File

Continuing with the example of the Si5345, when the values of P and M are fully represented by fractions (see Equation 2), by modifying the values of Mn, Md, Pn, and Pd, the desired end value of M÷P can be preserved. CBPro will try to find a new frequency plan that preserves all of the Fin and Fout requirements of the existing frequency plan in ways that will bypass the frequency offset issue.

$$Fout = Fin * \frac{Mn*Pd}{Md*Pn*N*R}$$ **Equation 2**

One effect of these changes is that the internal frequencies used at various points in the signal stream within the device will change. Users should review the CBPro suggested plan for possible issues:

- Loop Bandwidth: The new loop bandwidth selections are likely to be different.
- Hitless switching: If the new plan uses a fractional P value and the corresponding input frequency is < 300 MHz, then the hitless switching will no longer be compliant to ITU-T G.8262 recommendations.
- Fractional P and M dividers use slightly more power than when in integer mode.

6. Modify CBPro Frequency Plan Settings

If the suggested frequency plan from CBPro is not acceptable, it is possible in CBPro to allow the small frequency offset and generate a new project file (See Figure 11). This will result in a DRC warning. Other approaches are to examine the inputs to the multiplexer feeding into a DSPLL. It is possible that some inputs need not be precise and their values can be slightly adjusted to allow different frequency plan solutions to be found.

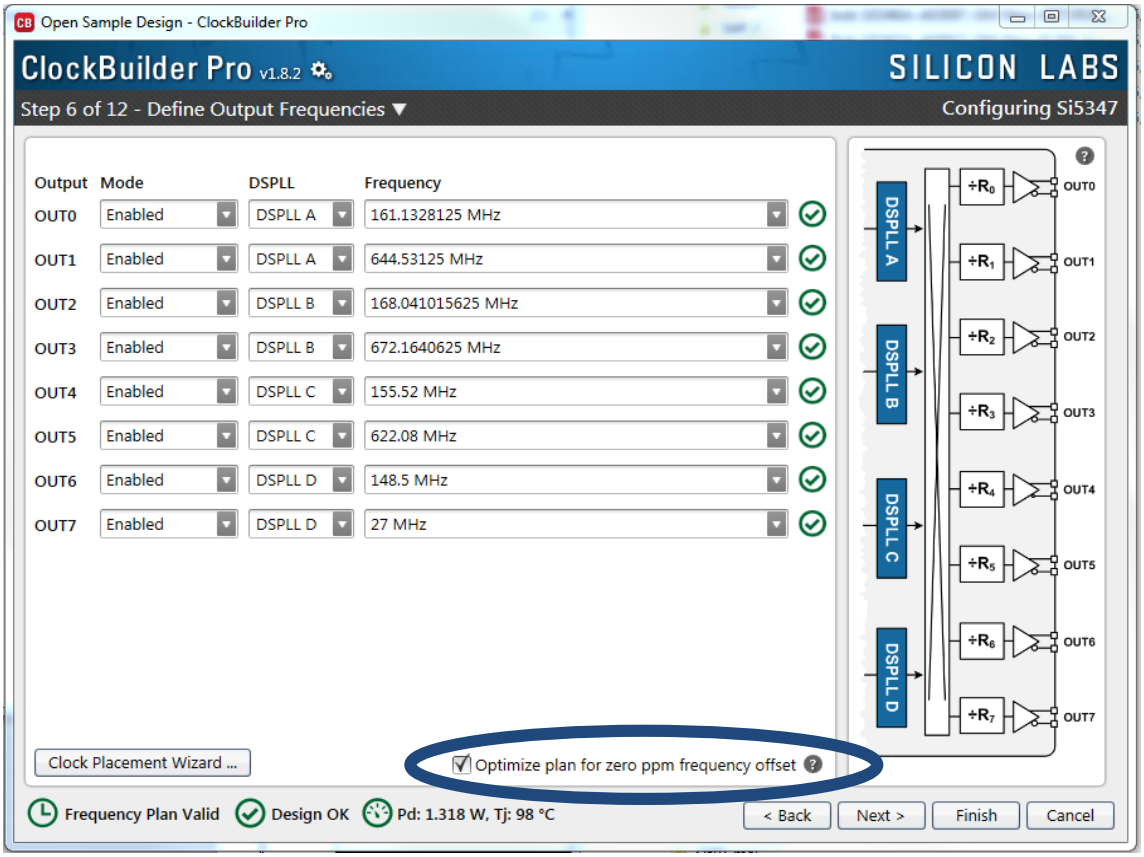


Figure 11 – Output Clock Selection

Issue	Cause	Possible Approaches to Work Around
Hitless switching no longer meets ITU-T G.8262	The associated input P divider became fractional and the input is < 300 MHz.	If the frequency offset is acceptable, choose the option to allow a frequency offset. This will restore the hitless switching performance.
Loop bandwidth is not acceptable	There are multiple possible signal paths the Phase Detector (PD), to eliminate the Frequency Offset issue, a lower PD frequency was required.	If the frequency offset is acceptable, choose the option to allow a frequency offset. This will restore the hitless switching performance.

7. For Users Who Don't Use CBPro

If your application does not use CBPro, please contact Silicon Labs' Applications Engineers directly (See Section 9).

8. Resolution

For applications that cannot tolerate the residual frequency offset issue, ClockBuilder Pro, beginning with v2.0, provides customers with an optional solution to the frequency offset issue. A future silicon revision will address the offset issue natively in silicon.

9. For Further Assistance

Contact the following Silicon Labs technical support for additional device-specific applications assistance.

10. Document Change List

Rev 1.3 to 1.4:

- Reformatted document (no other changes)

Rev 1.2 to 1.3:

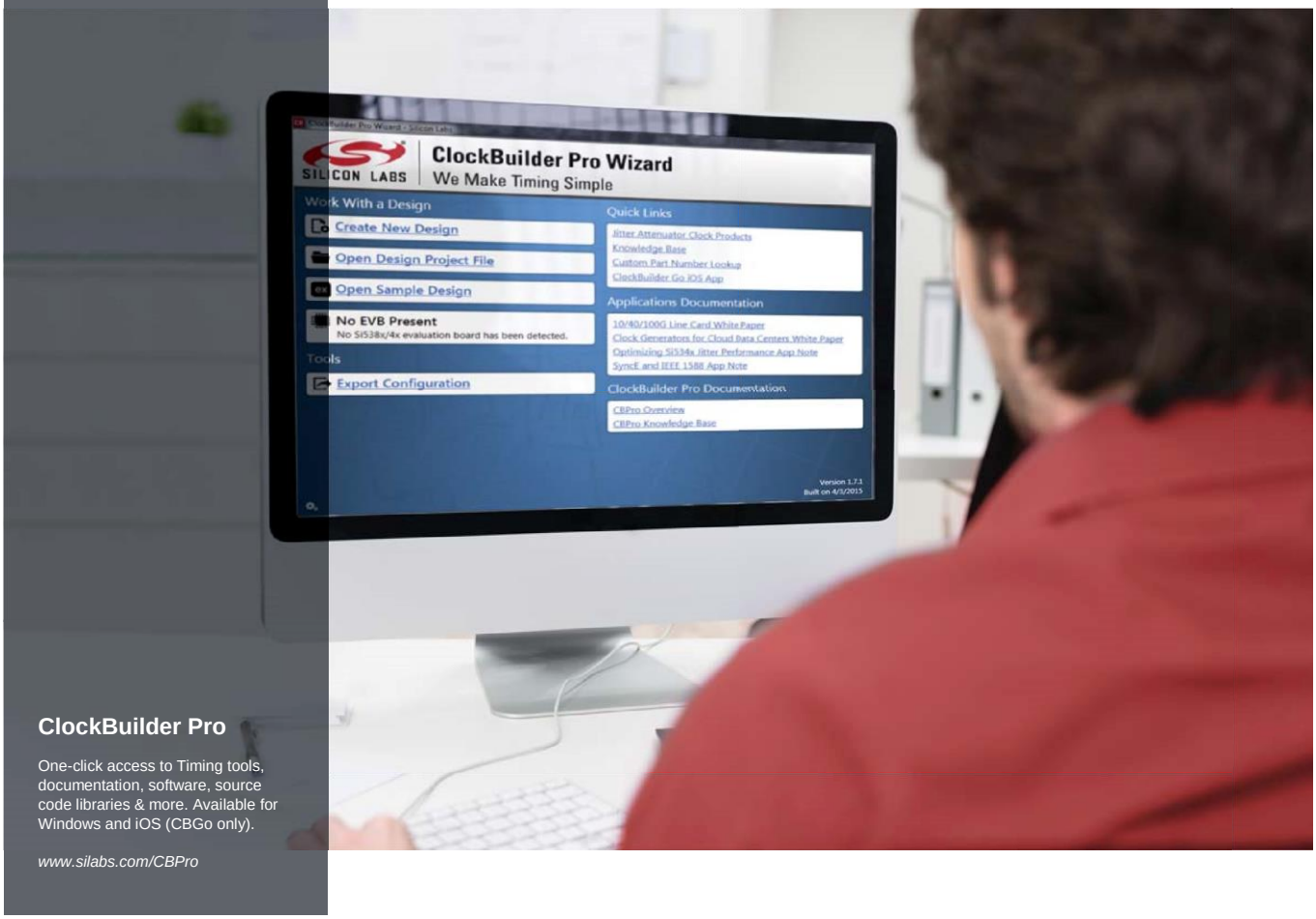
- Updated Figure 8

Rev 1.1 to 1.2:

- Section 3 has been re-written to improve the description of the options presented by CBPro

Rev 1.0 to Rev 1.1:

- Page 4: Fixed graphics offset
- Page 11 & 12, Corrected Figure 11 and Equations 1 and 2 by adding the missing "N" divider
- Page 14: Updated the contact information



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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