AK4191
Premium Digital ΔΣ Modulator

1. General Description

The AK4191 is a 7-bit Stereo Digital Delta-Sigma Modulator, achieving high quality sound reproduction. It corresponds to a 1536kHz PCM input and an DSD1024 input at maximum, suitable for playback of high resolution audio sources that are becoming widespread in Network Audio and USB-DACs Audio systems. In addition, it is capable of supporting a wide range of signals and achieving low out-of-band noise. The AK4191 has six types of digital filters, realizing simple and flexible sound reproduction in wide range of applications.

2. Features

- Digital Delta-Sigma Modulator
  - Selectable 5, 6 or 7-bits Modulator Data output
  - Four selectable types of Delta-Sigma Modulator Option
- 256×/128× Over Sampling
- Input Sampling Rate: 44.1 kHz to 1536 kHz (PCM, EXDF)
- 256×/128× Digital Filter
  - Ripple: ±0.001 dB, Attenuation: 150 dB (Sharp Roll-Off Filter Setting)
  - Six Types of High Quality Sound Filter Option
    - ・Short Delay Sharp Roll-off, GD = 9.0/fs
    - ・Short Delay Slow Roll-off, GD = 5.4/fs
    - ・Sharp Roll-off
    - ・Slow Roll-off
    - ・Super Slow Roll-off
    - ・Low Dispersion Short Delay Filter
    - ・Programmable Filter
- DSD64, DSD128, DSD256, DSD512, DSD1024 Input Support
  - Filter1 (fc = 19 kHz, DSD64 mode)
  - Filter2 (fc = 39 kHz, DSD64 mode)
- Digital De-emphasis for 32, 44.1 and 48 kHz sampling
- Soft Mute
- Digital Attenuator (0 dB to −127 dB, 0.5 dB step + mute)
- Multi-bit Delta-Sigma Modulator Data Input Interface
  - Volume (+6.0 dB to −127 dB, 0.5 dB step + mute)
- External Digital Filter Interface (EXDF Mode)
- Audio Input I/F Format
  - 64-bit Dual / 32-bit Single Input PCM I/F
    - MSB Justified
    - LSB Justified
    - I^2S
  - DSD
  - TDM
- PCM/DSD, EXDF/DSD Mode Automatic Mode Switching Function
- Data Synchronization to Master Clock
- Mono Mode

- Master Clock
  - 11.2896MHz/12.288MHz
- Register Control Mode with 4-wire Serial or I^2C interface
- Power Supply:
  - PVDD = 3.0 to 3.6 V
  - TVDD1/2/3/4 = 1.7 to 3.6 V
  - DVDD = 1.14 to 1.3 V
- Operational Temperature: −40 to 85 °C
- Digital Input Level: CMOS
- Package: 64-pin HTQFP

3. Table of Contents

1. General Description 1
2. Features 1
3. Table of Contents 3
4. Block Diagram and Functions 4
4.1. Block Diagram 4
4.2. Functions 5
5. Pin Configurations and Functions 6
5.1. Pin Configurations 6
5.2. Pin Functions 7
5.3. Handling of Unused Pins 9
6. Absolute Maximum Ratings 10
7. Recommended Operating Conditions 10
8. Electrical Characteristics 11
8.1. Digital Output Characteristics 11
8.2. Digital Filter Characteristics 13
8.3. DC Characteristics 31
8.4. Switching Characteristics 32
8.5. Timing Diagram 41
9. Functional Descriptions 49
9.1. Data Conversion Mode 49
9.2. System Clock 54
9.3. Audio Input Interface Format 60
9.4. Digital Filter 75
9.5. De-emphasis Filter (PCM Mode) 77
9.6. Digital Attenuator 78
9.7. Gain Adjustment Function 79
9.8. Zero Detection, DSD Full-scale Detection 80
9.9. LR Channel Output Signal Select, Phase Inversion Function 84
9.10. Automatic Data Conversion Mode Switching 85
9.11. Soft Mute Function 93
9.12. MUTEN output 94
9.13. MBD zero output 94
9.14. DSM Data Mix Function 95
9.15. MCLKO output 95
9.16. Delta-Sigma Modulator 97
9.17. Power Up/Down Sequence 98
9.18. Internal State 102
9.19. Clock Synchronize Function (PCM Mode, EXDF Mode) 106
9.20. Control Interface 108
9.21. Register Map 115
9.22. Register Definitions 116
10. Recommended External Circuits 125
10.1. External Connection Example 125
10.2. Grounding and Power Supply Decoupling 126
11. Package 127
11.1. Outline Dimensions: HTQFP64-10x10-0.5 127
11.2. Material & Terminal Finish 128
11.3. Marking 128
12. Revision Histroy 129

4. Block Diagram and Functions

4.1. Block Diagram

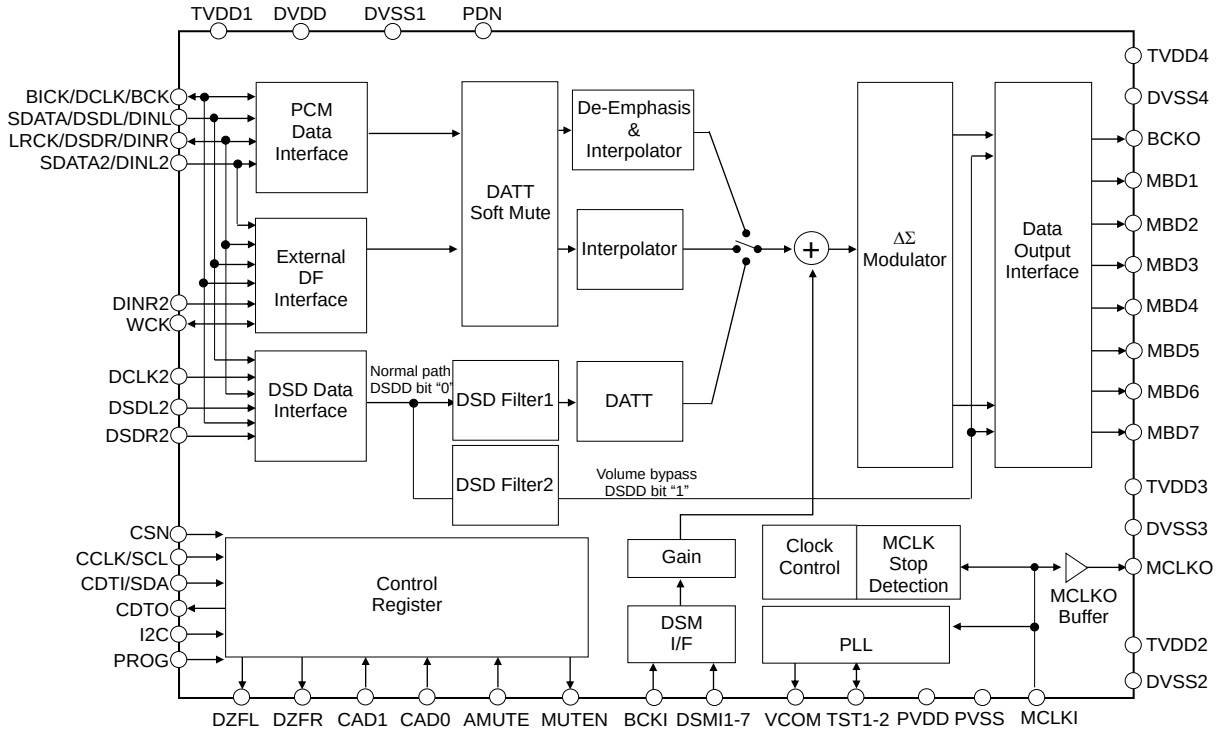


Figure 1. AK4191 Block Diagram1 (Synchronous Mode)

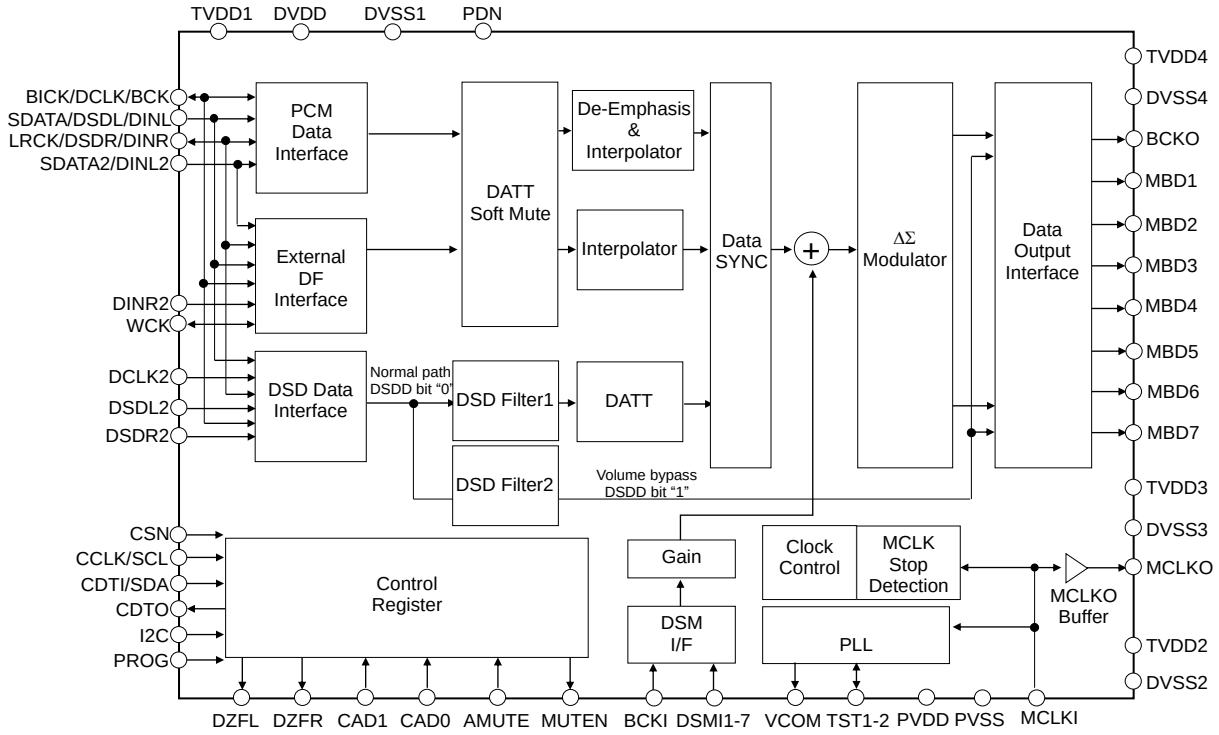


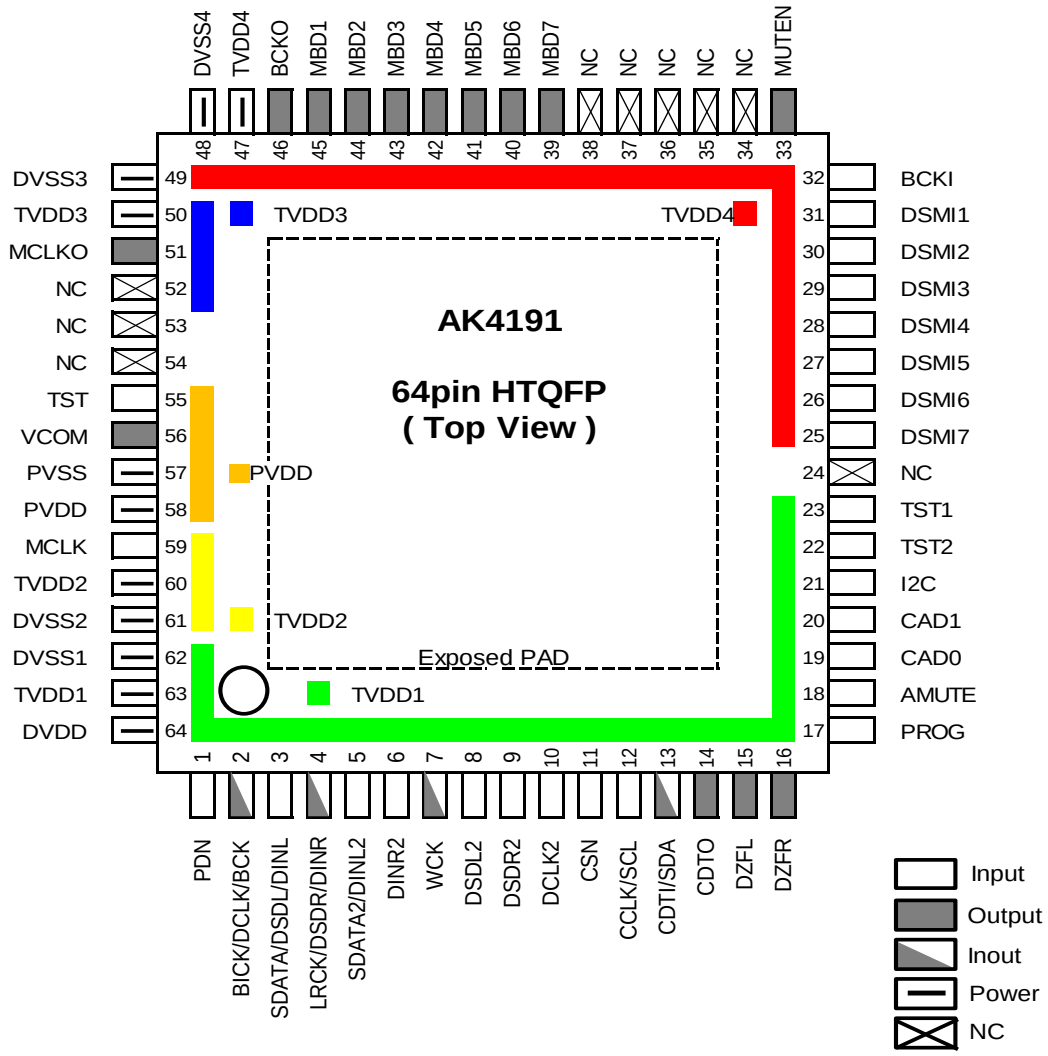
Figure 2. AK4191 Block Diagram2 (Asynchronous Mode)

4.2. Functions

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDATA, SDATA2 input data by synchronizing with LRCK and BICK.
External DF Interface	Receive external digital filter outputs. Execute serial/parallel conversion of DINL/L2 and DINR/R2 input data by synchronizing with BCK.
DSD Data Interface	1-bit data that is input from DSDL and DSDR pins is received by synchronizing with DCLK.
DSD Filter 1/2	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
ΔΣ Modulator	Output multi-bit data to Analog-DAC. This block is four selectable types of delta-sigma modulators.
Control Register	Internal register keep its settings for each mode. Control registers are accessed in 4-wire (CSN, CCLK, CDTI, CDTO) or I2C-Bus (SCL, SDA) control mode.
PLL	Generates internal master clock from the input clock of the MCLK pin.
Clock Control	Divide internal master clock. In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by ADCKS bit
MCLK Stop Detection	Detects when the master clock input is absent.
MCLKO Buffer	MCLKO level shifter.
Data SYNC	Data synchronization block
DSM I/F	Multi-bit Delta-Sigma data that is input from DSMI7-1 pins is received by synchronizing with BCKI.
Gain	Apply Gain Control process to Multi-bit Delta-Sigma Input data

5. Pin Configurations and Functions

5.1. Pin Configurations



Note 1: The exposed pad on the bottom surface of the package should be connected to PVSS.

5.2. Pin Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State (PDN = "L")
1	PDN	I	TVDD1/DVSS1	Power-Up, Power-Down Pin When at "L", the AK4191 is in power-down mode. The AK4191 must always be in power-down mode upon power on.	Hi-Z
2	BICK	I/O	TVDD1/DVSS1	Audio Serial Data Clock Pin in PCM mode	Pull-down to DVSS1 (46 kΩ, typ)
	BCK	I/O		Audio Serial Data Clock Pin in EXDF mode	
	DCLK	I		Audio Serial Data Clock Pin in DSD mode (@DSDPATH bit = "1")	
3	SDATA	I	TVDD1/DVSS1	Audio Serial Data Input Pin in PCM mode	Hi-Z
	DINL	I		Audio Serial Data Input Pin in EXDF mode	
	DSDL	I		Audio Serial Data Input Pin in DSD mode (@DSDPATH bit = "1")	
4	LRCK	I/O	TVDD1/DVSS1	Input Channel Clock pin in PCM mode	Pull-down to DVSS1 (46 kΩ, typ)
	DINR	I		Audio Serial Data Input Pin in EXDF mode	
	DSDR	I		Audio Serial Data Input Pin in DSD mode (@DSDPATH bit = "1")	
5	SDATA2	I	TVDD1/DVSS1	Audio Serial Data Input pin in PCM mode	Hi-Z
	DINL2	I		Audio Serial Data Input pin in EXDF mode (@DSDPATH bit = "1")	
6	DINR2	I	TVDD1/DVSS1	Audio Serial Data Input pin in EXDF mode	Hi-Z
7	WCK	I/O	TVDD1/DVSS1	Word Clock input pin in EXDF mode	Pull-down to DVSS1 (46 kΩ, typ)
8	DSDL2	I	TVDD1/DVSS1	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = "0")	Hi-Z
9	DSDR2	I	TVDD1/DVSS1	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = "0")	Hi-Z
10	DCLK2	I	TVDD1/DVSS1	DSD Clock pin in DSD mode (@DSDPATH bit = "0")	Hi-Z
11	CSN	I	TVDD1/DVSS1	Chip Select pin in 4-wire serial Register Control mode	Hi-Z
12	CCLK	I	TVDD1/DVSS1	Control Data Clock pin in 4-wire serial Register Control mode	Hi-Z
	SCL	I		Control Data Clock Input pin in I^2C Bus Register Control mode	
13	CDTI	I	TVDD1/DVSS1	Control Data Input pin in 4-wire serial Register Control mode	Hi-Z
	SDA	I/O		Control Data Input pin in I^2C Bus Register Control mode	
14	CDTO	O	TVDD1/DVSS1	Control Data Output pin in 4-wire serial Register Control mode	Hi-Z
15	DZFL	O	TVDD1/DVSS1	Lch Zero Input Detect pin	"L" Output
16	DZFR	O	TVDD1/DVSS1	Rch Zero Input Detect pin	"L" Output
17	PROG	I	TVDD1/DVSS1	Programmable Filter Coefficient Setting Enable	Hi-Z

No.	Pin Name	I/O	Protection Diode	Function	Power Down State (PDN = "L")
18	AMUTE	I	TVDD1/DVSS1	MUTE Control for External Analog-DAC	Hi-Z
19	CAD0	I	TVDD1/DVSS1	Chip Address 0 pin	Hi-Z
20	CAD1	I	TVDD1/DVSS1	Chip Address 1 pin	Hi-Z
21	I2C	I	TVDD1/DVSS1	Serial Control Interface Select pin. "L": 4-wire serial control interface. "H": I^2C Bus control interface.	Hi-Z
22	TST2	I	TVDD1/DVSS1	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS1 (46 kΩ, typ)
23	TST1	I	TVDD1/DVSS1	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS1 (46 kΩ, typ)
24	NC	-	-	No internal bonding. Connect to PVSS	-
25	DSMI7	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
26	DSMI6	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
27	DSMI5	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
28	DSMI4	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
29	DSMI3	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
30	DSMI2	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
31	DSMI1	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
32	BCKI	I	TVDD4/DVSS4	Digital Audio Clock Input Pin	Hi-Z
33	MUTEN	O	TVDD4/DVSS4	MUTEN Output for Analog-DAC	"L" Output
34-38	NC	-	-	No internal bonding. Connect to PVSS	-
39	MBD7	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
40	MBD6	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
41	MBD5	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
42	MBD4	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
43	MBD3	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
44	MBD2	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
45	MBD1	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
46	BCKO	O	TVDD4/DVSS4	Digital Audio Data Clock Output Pin	"L" Output

No.	Pin Name	I/O	Protection Diode	Function	Power Down State (PDN = "L")
47	TVDD4	-	-	Digital Output Power Supply Pin, TVDD4 = TVDD3 − 0.1 V to TVDD3 + 0.1 V	-
48	DVSS4	-	-	Digital Ground Pin	-
49	DVSS3	-	-	Digital Ground Pin	-
50	TVDD3	-	-	MCLKO Output Power Supply Pin, TVDD3 = 1.7 to 3.6 V	-
51	MCLKO	O	TVDD3/DVSS3	MCLK Output Pin	Pull-down to DVSS3 (46 kΩ, typ)
52-54	NC	-	-	No internal bonding. Connect to PVSS	-
55	TST	I	PVDD/PVSS	Connect to PVSS	Hi-z
56	VCOM	O	PVDD/PVSS	Analog Block Common Voltage Output. Connect 2.2μF capacitor between this pin and PVSS. This pin must not be connected to external circuit.	Pull-down to PVSS (500 Ω, typ)
57	PVSS	-	-	Analog Ground Pin	-
58	PVDD	-	-	Analog Power Supply Pin, PVDD = 3.0 to 3.6 V	-
59	MCLK	I	TVDD2/DVSS2	MCLK Input pin	Hi-Z
60	TVDD2	-	-	Digital Power Supply Pin, TVDD2 = 1.7 to 3.6 V	-
61	DVSS2	-	-	Digital Ground Pin	-
62	DVSS1	-	-	Digital Ground Pin	-
63	TVDD1	-	-	Digital Power Supply Pin, TVDD1 = 1.7 to 3.6 V	-
64	DVDD	-	-	1.2V Power Input Pin	-
Exposed PAD		-	-	No internal bonding. Connect to PVSS	-

5.3. Handling of Unused Pins

Classification	Pin Name	Setting
Digital Output	CDTO	Connect to DVSS1 or TVDD1
	DZFL, DZFR	Open
	MBD1, MBD2	Open
	MUTEN	Open
	MCLKO	Open
Digital Input	SDATA2/DINL2, DINR2, WCK	Connect to DVSS1
	DSDL2, DSDR2, DCLK2	Connect to DVSS1
	CSN	Connect to DVSS1
	PROG	Connect to DVSS1
	AMUTE	Connect to DVSS1
	BCKI, DSMI7-1	Connect to DVSS4

6. Absolute Maximum Ratings

(PVSS = DVSS 1/2/3/4 = 0 V; (Note 2))

Parameter		Symbol	Min	Max	Unit
Power Supplies	PLL	PVDD	−0.3	4.3	V
	Digital I/O	TVDD1	−0.3	4.3	V
	Clock Interface	TVDD2	−0.3	4.3	V
	MCLKO Output	TVDD3	−0.3	4.3	V
	Digital Output	TVDD4	−0.3	4.3	V
	Digital Core	DVDD	−0.3	1.4	V
	|PVSS−DVSS1|, |PVSS−DVSS2|, |PVSS−DVSS3|, |PVSS−DVSS4|, |DVSS2−DVSS1|, |DVSS3−DVSS1|, |DVSS3−DVSS2| |DVSS4−DVSS1|, |DVSS4−DVSS2|, |DVSS4−DVSS3| (Note 2)	ΔGND	0	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 3)		VIND	−0.3	TVDD1+0.3 or 4.3	V
MCLK Input Voltage (Note 3)		VINCK	−0.3	TVDD2+0.3 or 4.3	V
Ambient Temperature (Power Supplied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages are with respect to ground.

Note 3. PVSS and DVSS1/2/3/4 must be connected to the same analog ground plane. The exposed pad on the bottom surface of the package must be connected to PVSS.
Maximum input voltage of Digital Input Voltage is lower value between (TVDD1 + 0.3) V and 4.3 V. Same as, Maximum input voltage of MCLK Input Voltage is lower value between (TVDD2 + 0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(PVSS = DVSS1/2/3/4 = 0 V; Note 2)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	PLL	PVDD	3.0	3.3	3.6	V
	Digital I/O	TVDD1	1.7	1.8	3.6	V
	Clock Interface	TVDD2	1.7	1.8	3.6	V
	MCLKO Output	TVDD3	1.7	1.8	3.6	V
	Digital Output	TVDD4	TVDD3−0.1	TVDD3	TVDD3+0.1	V
	Digital Core	DVDD	1.14	1.2	1.3	V

Note 4. DVDD must be supplied at the same time as or after TVDD1/2/3/4. The power up sequence between PVDD, TVDD1, TVDD2, TVDD3 and TVDD4 is not critical.

Note 5. Do not turn off the TVDD1 power supply of the AK4191 with the power supply of the surrounding device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD1 or less voltage.

*** AKM assumes no responsibility for the usage beyond the conditions in this data sheet.**

8. Electrical Characteristics

8.1. Digital Output Characteristics

8.1.1. PCM Mode

(Ta = −40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V, PVSS = DVSS1/2/3/4 = 0 V; fs = 44.1 kHz; BICK = 64fs; Signal Frequency = 1 kHz; 32-bit Input data; Measurement bandwidth = 20 Hz to 20 kHz; OSR = 256fs mode (OSR bit = "0"); Output bit length = 7 (OBIT[1:0] bits = "00"); Output Gain = 56% (GC[3:0] bits = "0000"); Cload = 20 pF unless otherwise specified.)

Parameter		Min	Typ	Max	Unit
Resolution		-	-	64	Bit
Dynamic Characteristics					
THD+N (Synchronous mode)					
0dBFS	BW = 20 kHz	-	−153	-	dB
	BW = 40 kHz	-	−145	-	dB
	BW = 80 kHz	-	−138	-	dB
	BW = 160 kHz	-	−131	-	dB
THD+N (Asynchronous mode)					
0dBFS	BW = 20 kHz	-	−153	-	dB
	BW = 40 kHz	-	−145	-	dB
	BW = 80 kHz	-	−138	-	dB
	BW = 160 kHz	-	−131	-	dB
Dynamic Range (−60dBFS, A-weighted)		-	156	-	dB
S/N (No Filter)	GC [3:0] = "0000"	-	153	-	dB
S/N (A-weighted)	GC [3:0] = "0000"	-	156	-	dB
	GC [3:0] = "0100"	-	158	-	dB
Power Supplies					
Power Supply Current					
Normal operation (PDN pin = "H")					
PVDD		1	2	3	mA
TVDD1 (typ 1.8 V)		-	0.1	1.5	mA
TVDD2 (typ 1.8 V)		-	0.1	0.3	mA
TVDD3 (typ 1.8 V)		-	0.2	2	mA
TVDD4 (typ 1.8 V)		-	1.5	9	mA
DVDD					
	fs = 44.1 kHz	-	13	24	mA
	fs = 96 kHz	-	24	41	mA
	fs = 192 kHz	-	42	67	mA
	fs = 384 kHz	-	25	41	mA
	fs = 768 kHz	-	43	68	mA
	fs = 1536 kHz	-	15	28	mA
Power down (PDN pin = "L") (Note 6) PVDD+TVDD1+TVDD2+TVDD3+TVDD4+DVDD		-	400	-	μA

Note 6. In power down mode, all digital input pins including clock pins (MCLK, BICK, BCKI and LRCK) are held to DVSS1, DVSS2 or DVSS4.

8.1.2. DSD Mode

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V, PVSS = DVSS1/2/3/4 = 0 V; Signal Frequency = 1 kHz; Measurement bandwidth = 20 Hz to 20 kHz; OSR = 256fs mode (OSR bit = "0"); Output bit length = 7 (OBIT[1:0] bits = "00"); Output Gain = 56% (GC[3:0] bits = "0000") unless otherwise specified.)

Parameter		Min	Typ	Max	Unit
Dynamic Characteristics					
THD+N (Synchronous mode)					
0dB input (Note 7)	DSD64	-	–116	-	dB
	DSD128	-	–119	-	dB
	DSD256	-	–124	-	dB
	DSD512	-	–131	-	dB
	DSD1024	-	–140	-	dB
THD+N (Asynchronous mode)					
0dB input (Note 7) Base Frequency: 44.1 kHz to 48 kHz	DSD64	-	–116	-	dB
	DSD128	-	–119	-	dB
	DSD256	-	–124	-	dB
	DSD512	-	–131	-	dB
	DSD1024	-	–140	-	dB
0dB input (Note 7) Base Frequency: 48 kHz to 44.1 kHz	DSD64	-	–116	-	dB
	DSD128	-	–119	-	dB
	DSD256	-	–124	-	dB
	DSD512	-	–131	-	dB
	DSD1024	-	–135	-	dB
S/N					
Digital "0" input (Note 8Note 7)	No filter	-	153	-	dB
	A-weighted	-	156	-	dB
Power Supplies					
Power Supply Current					
Normal operation (PDN pin = "H")					
PVDD		1	2	3	mA
TVDD1 (typ 1.8 V)		-	0.1	1.5	mA
TVDD2 (typ 1.8 V)		-	0.1	0.3	mA
TVDD3 (typ 1.8 V)		-	0.2	2	mA
TVDD4 (typ 1.8 V)		-	1.5	9	mA
DVDD	DSD64	-	7	-	mA
	DSD128	-	7.5	-	mA
	DSD256	-	8	-	mA
	DSD512	-	10.5	-	mA
	DSD1024	-	13.5	-	mA

Note 7. The output level is assumed as 0dB when a 1 kHz 25% to 75% duty sine wave is input. Pop noise may occur if the input signal exceeds 0dB.

Note 8. Digital "0" is a "01101001" digital zero code pattern.

8.2. Digital Filter Characteristics

8.2.1. Sharp Roll-Off Filter Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; DEM = OFF; SD bit = "0", SLOW bit = "0", SSLOW bit = "0"; unless otherwise specified)

▪ 1×/2×/4× Speed Mode (PCM mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	–0.02 dB	-	0	-	0.4535fs	kHz
	–6.0 dB	-	-	0.4898fs	-	kHz
Pass band		PB	0	-	0.4535fs	kHz
Stop band		SB	0.5465fs	-	-	kHz
Pass band Ripple	(Note 10)	PR	-	-	±0.001	dB
Stop band Attenuation	(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	1× Speed Mode	GD	-	41.7	-	1/fs
	2× Speed Mode	GD	-	41.7	-	1/fs
	4× Speed Mode	GD	-	41.4	-	1/fs

▪ 8×/16× Speed Mode (PCM and EXDF mode)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	–0.4 dB	-	0	-	0.4535fs	kHz
	–6.0 dB	-	-	0.4901fs	-	kHz
Pass band		PB	0	-	0.4535fs	kHz
Stop band		SB	0.5465fs	-	-	kHz
Pass band Ripple	(Note 10)	PR	-	-	±0.001	dB
Stop band Attenuation	(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	8× Speed Mode	GD	-	43.5	-	1/fs
	16× Speed Mode	GD	-	42.4	-	1/fs

▪ 32× Speed Mode (PCM and EXDF mode) (Note 12)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	–1 dB	-	0	-	0.3242fs	kHz
	–6.0 dB	-	-	0.4708fs	-	kHz
Pass band		PB	0	-	0.3242fs	kHz
Stop band		SB	0.8548fs	-	-	kHz
Pass band Ripple	(Note 10)	PR	-	-	±0.001	dB
Stop band Attenuation	(Note 9)	SA	150	-	-	dB
Group Delay	(Note 11)	GD	-	10.9	-	1/fs

Note 9. Frequency response refers to the output level of 1 kHz. Stopband attenuation band ranges from SB to fs.

Note 10. This value is the gain amplitude in pass band width.

Note 11. The calculating delay time which occurred by digital filtering. This value is from setting the 16/20/24/32 bit data of both channels to the MBD7-1 output.

Note 12. In 32× speed mode, the digital filter mode is limited to Sharp Roll-Off Filter mode.

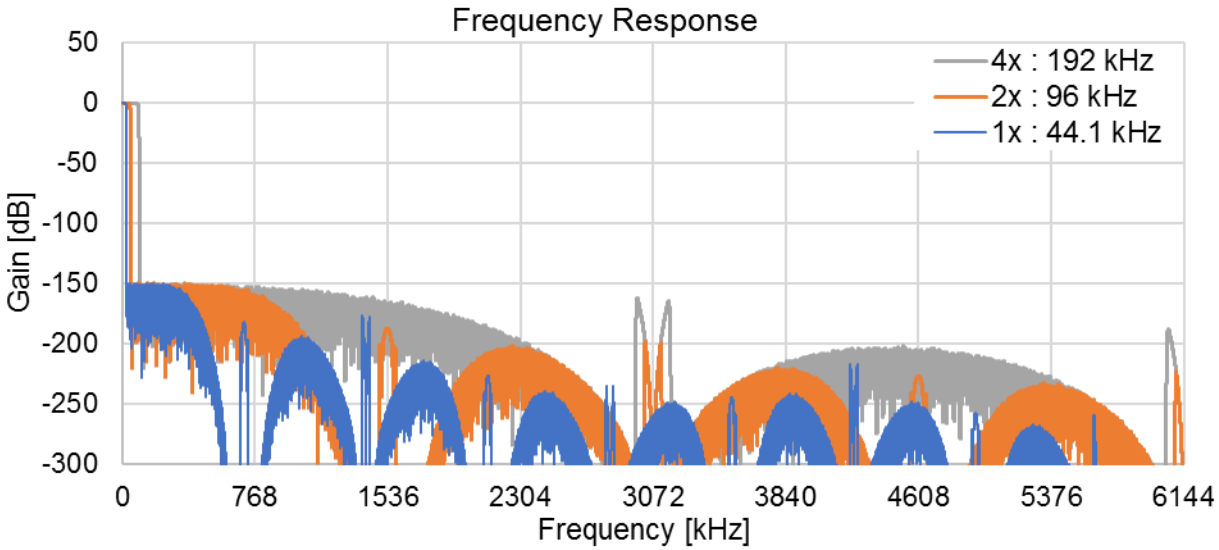


Figure 3. Sharp Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 6.144MHz)

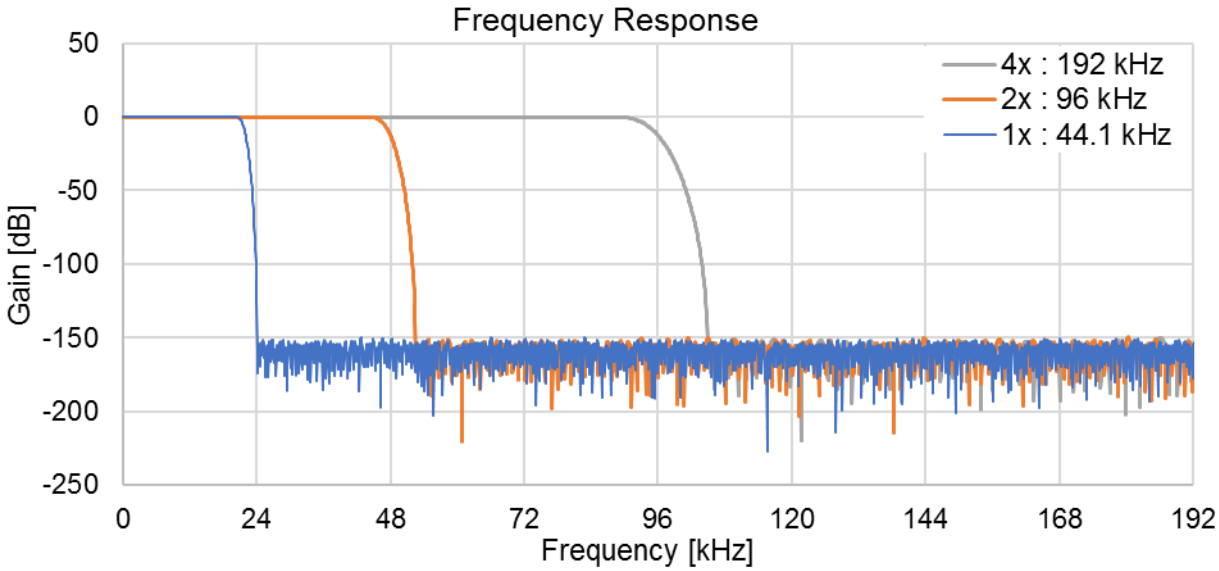


Figure 4. Sharp Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 192kHz)

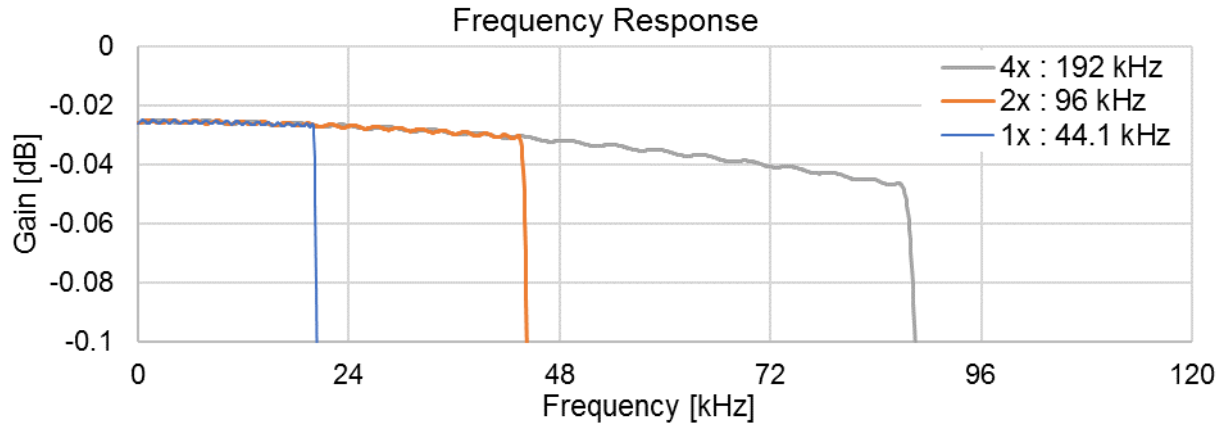


Figure 5. Sharp Roll-Off Filter Pass Band Ripple (1×/2×/4× Speed Mode)

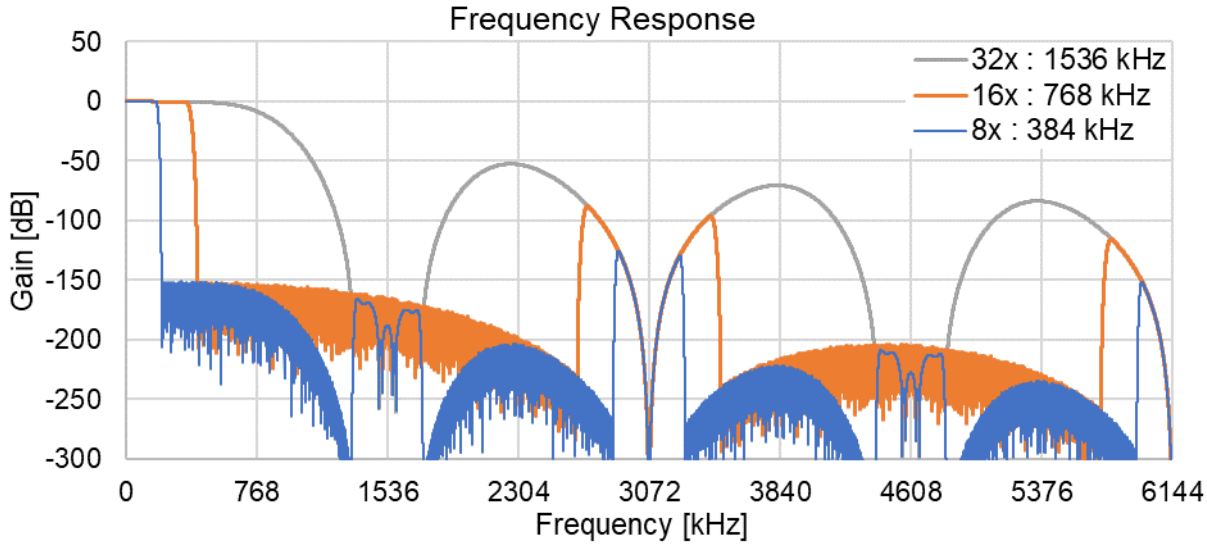


Figure 6. Sharp Roll-Off Filter Frequency Response (8×/16×/32× Speed Mode; to 6.144MHz)

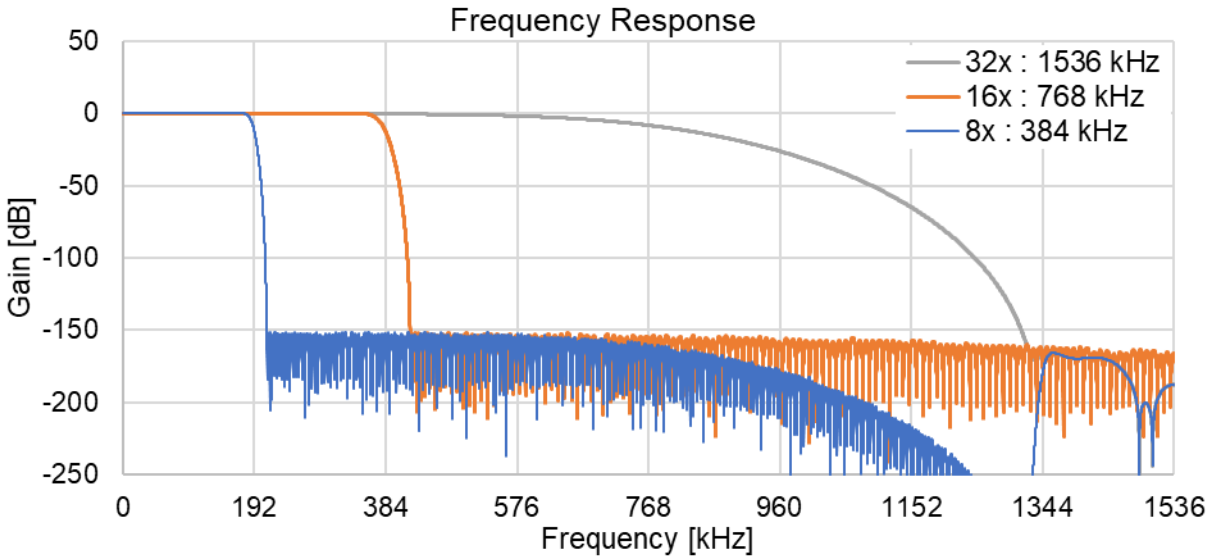


Figure 7. Sharp Roll-Off Filter Frequency Response (8×/16×/32× Speed Mode; to 1536kHz)

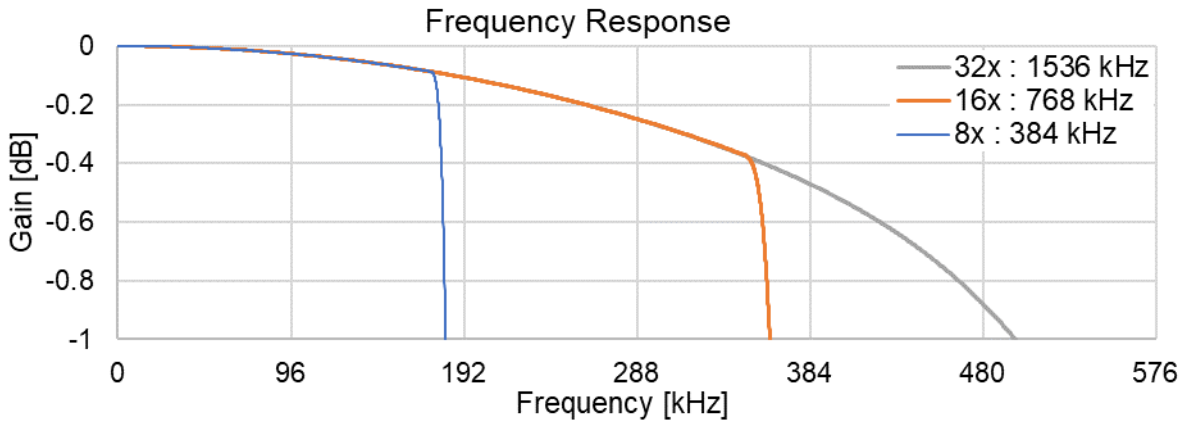


Figure 8. Sharp Roll-Off Filter Pass Band Ripple (8×/16×/32× Speed Mode)

8.2.2. Slow Roll-Off Filter Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; DEM = OFF; SD bit = "0", SLOW bit = "1", SSLOW bit = "0"; unless otherwise specified)

▪ **1×/2×/4× Speed Mode (PCM mode)**

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.02 dB	-	0	-	0.1814fs	kHz
		–6.0 dB	-	-	0.4207fs	-	kHz
Pass band			PB	0	-	0.1814fs	kHz
Stop band			SB	0.8fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.01	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	1× Speed Mode		GD	-	7.0	-	1/fs
	2× Speed Mode		GD	-	7.0	-	1/fs
	4× Speed Mode		GD	-	6.8	-	1/fs

▪ **8×/16× Speed Mode (PCM and EXDF mode)**

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.1 dB	-	0	-	0.1836fs	kHz
		–6.0 dB	-	-	0.4195fs	-	kHz
Pass band			PB	0	-	0.1836s	kHz
Stop band			SB	0.888fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.01	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	8× Speed Mode		GD	-	8.9	-	1/fs
	16× Speed Mode		GD	-	7.8	-	1/fs

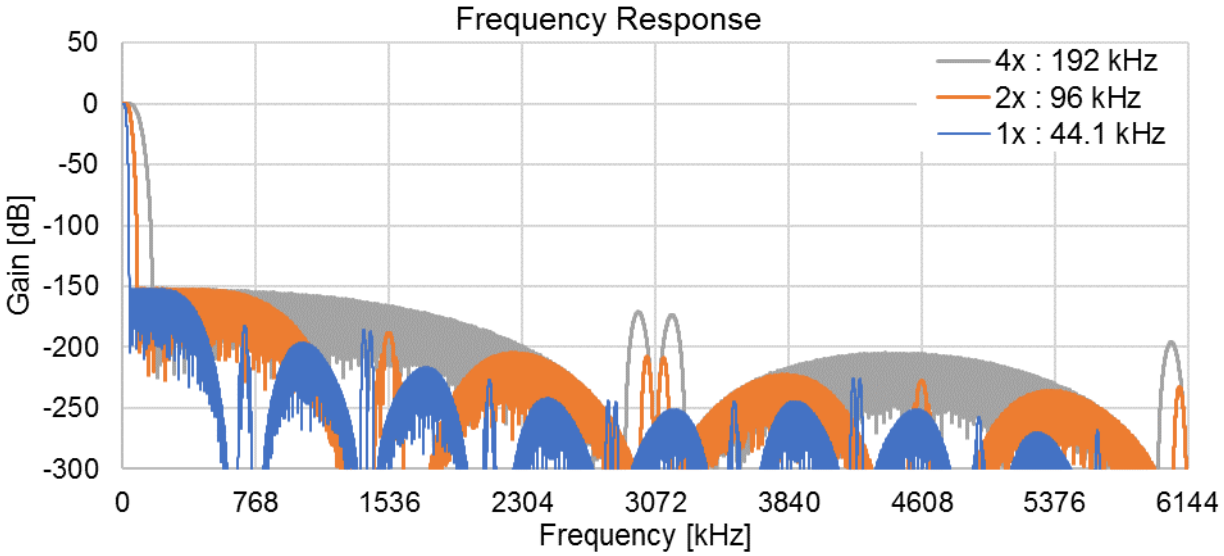


Figure 9. Slow Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 6.144MHz)

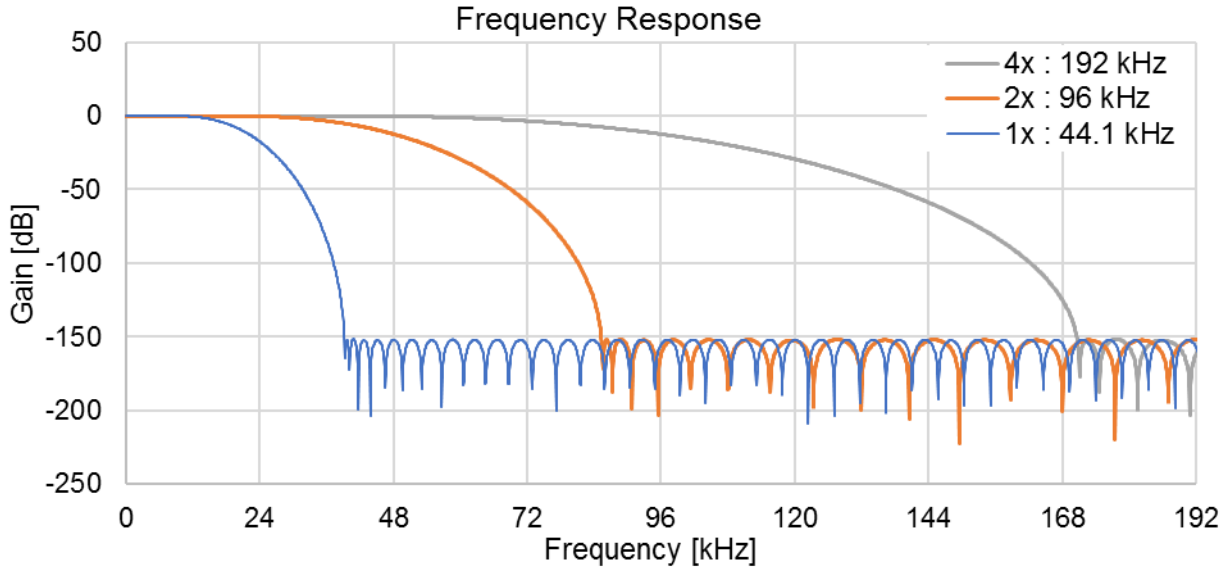


Figure 10. Slow Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 192kHz)

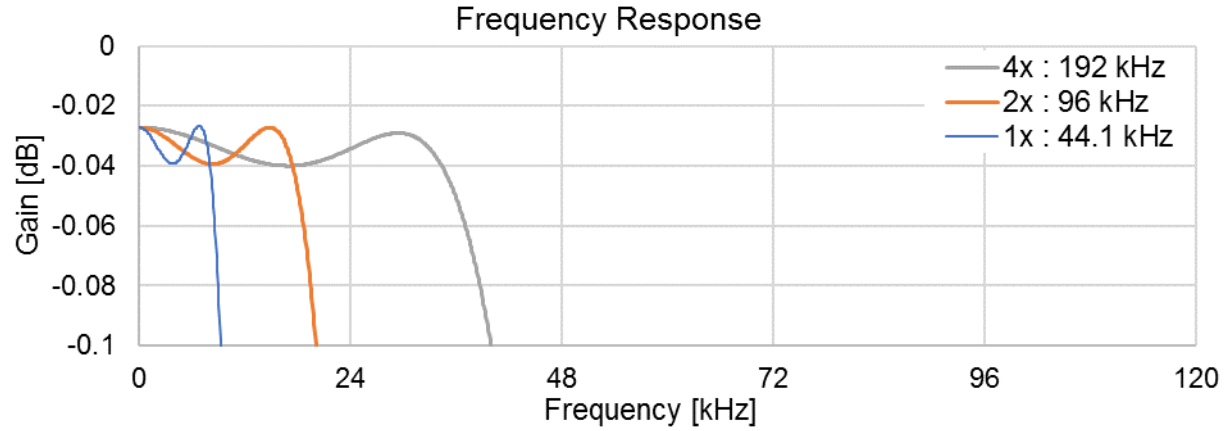


Figure 11. Slow Roll-Off Filter Pass Band Ripple (1×/2×/4× Speed Mode)

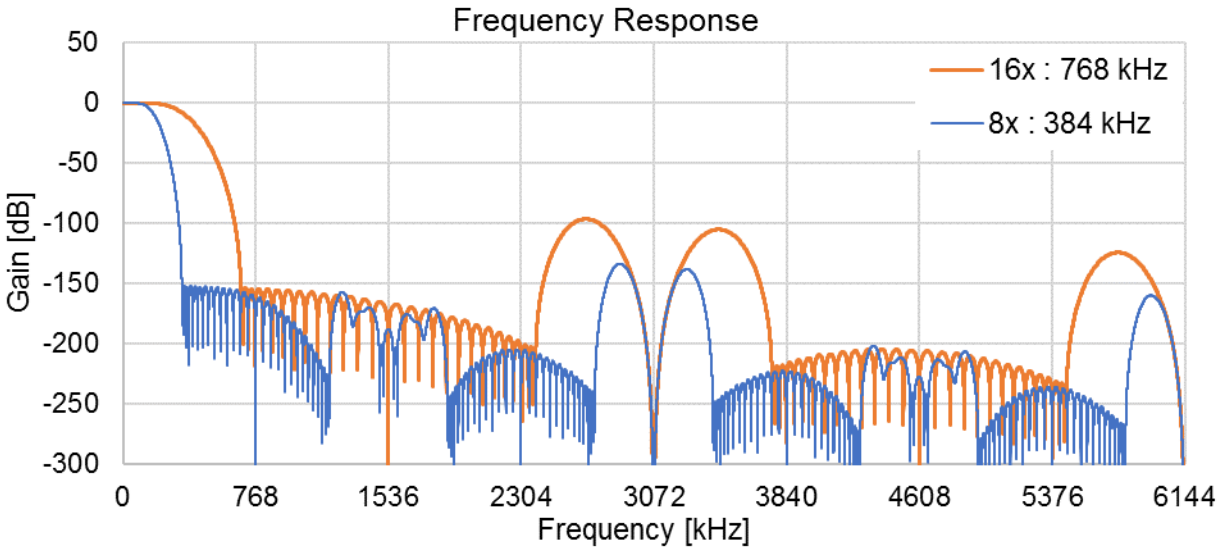


Figure 12. Slow Roll-Off Filter Frequency Response (8×/16× Speed Mode; to 6.144MHz)

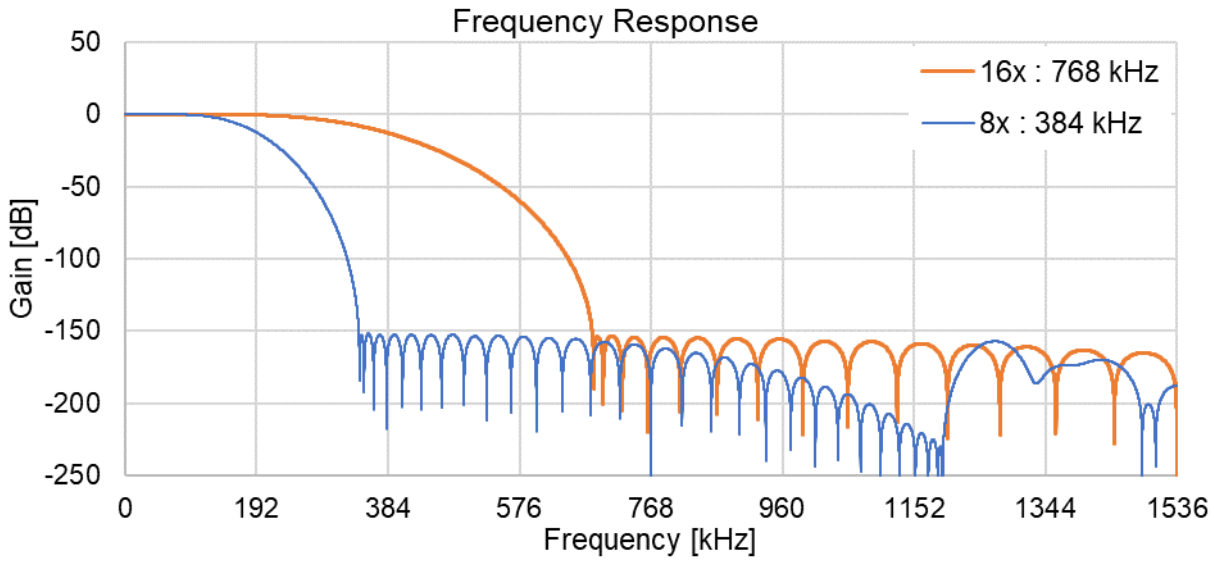


Figure 13. Slow Roll-Off Filter Frequency Response (8×/16× Speed Mode; to 1536kHz)

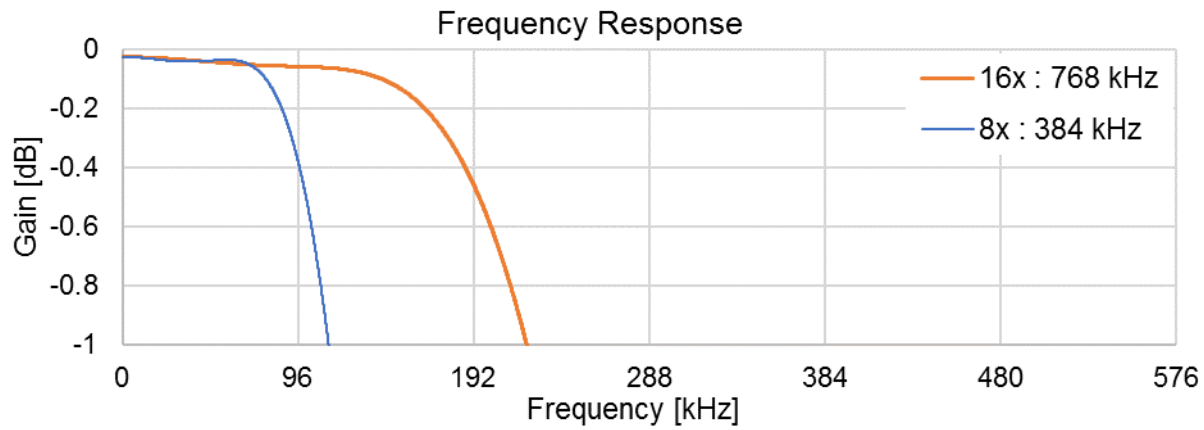


Figure 14. Slow Roll-Off Filter Pass Band Ripple (8×/16× Speed Mode)

8.2.3. Short Delay Sharp Roll-Off Filter Characteristics

(Ta = -40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; DEM = OFF; SD bit = "1", SLOW bit = "0", SSLOW bit = "0"; unless otherwise specified)

▪ 1×/2×/4× Speed Mode (PCM mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		−0.02 dB	-	0	-	0.4535fs	kHz
		−6.0 dB	-	-	0.4898fs	-	kHz
Pass band			PB	0	-	0.4535fs	kHz
Stop band			SB	0.5465fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.001	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	1× Speed Mode		GD	-	9.0	-	1/fs
	2× Speed Mode		GD	-	9.0	-	1/fs
	4× Speed Mode		GD	-	8.7	-	1/fs

▪ 8×/16× Speed Mode (PCM and EXDF mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		−0.4 dB	-	0	-	0.4535fs	kHz
		−6.0 dB	-	-	0.4894fs	-	kHz
Pass band			PB	0	-	0.4535fs	kHz
Stop band			SB	0.5465fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.001	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	8× Speed Mode		GD	-	8.4	-	1/fs
	16× Speed Mode		GD	-	7.3	-	1/fs

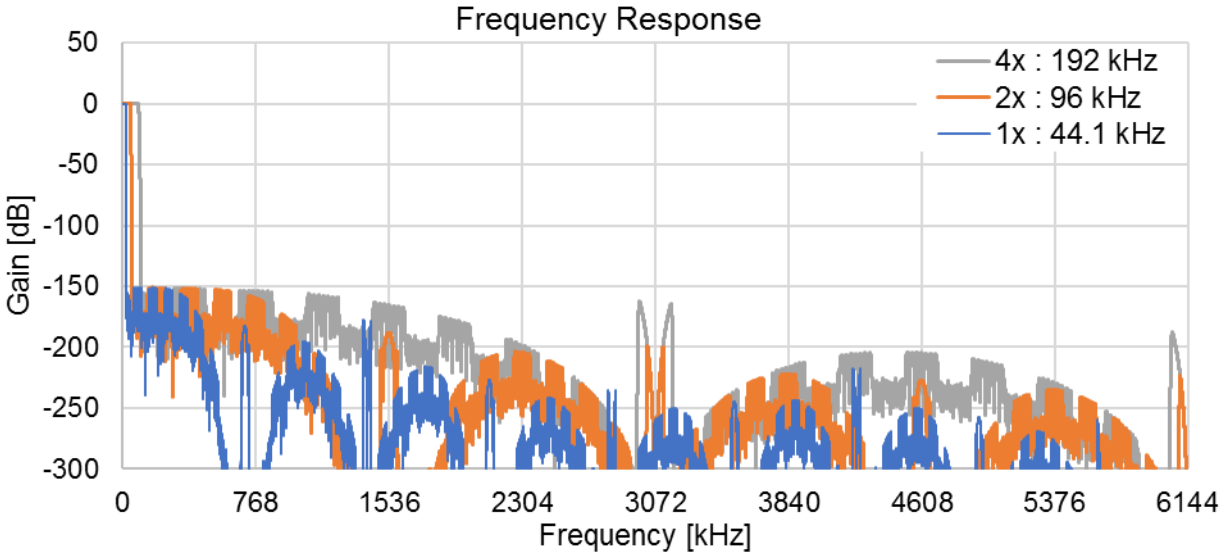


Figure 15. Short Delay Sharp Roll-Off Filter Frequency Response
(1×/2×/4× Speed Mode; to 6.144MHz)

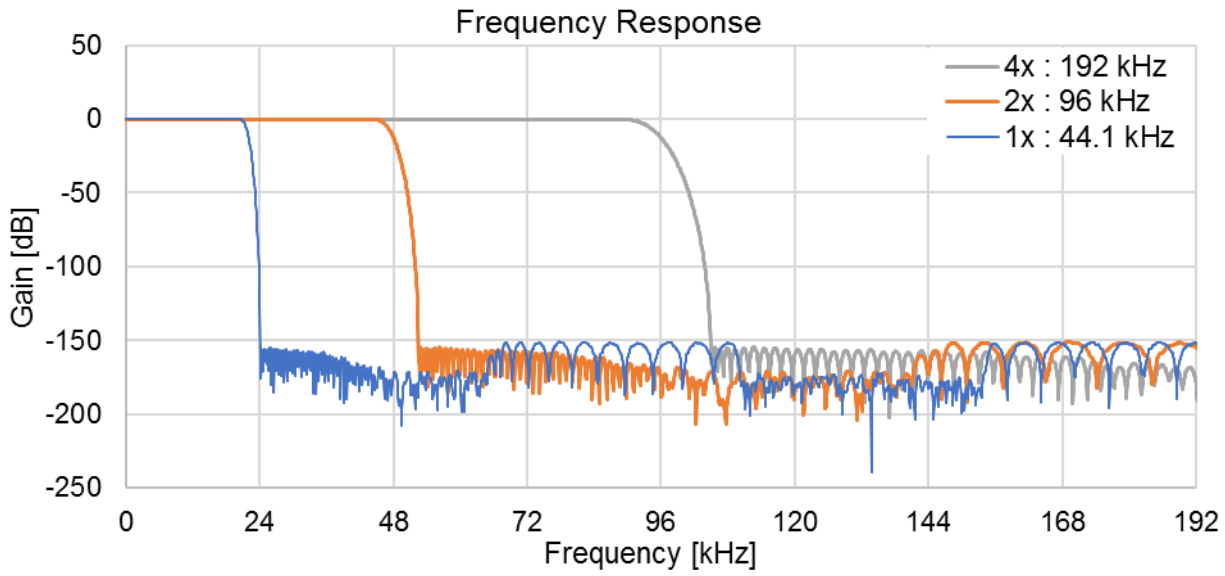


Figure 16. Short Delay Sharp Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 192kHz)

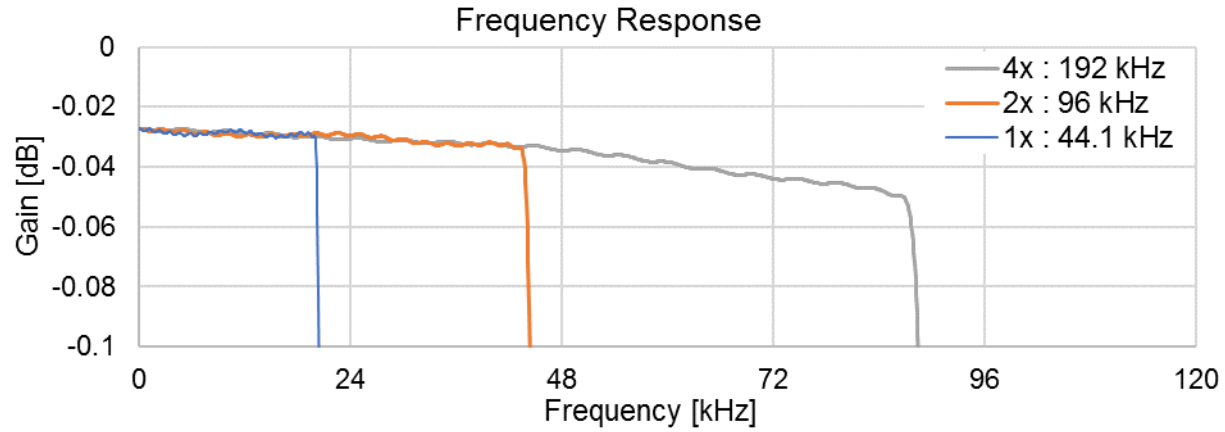


Figure 17. Short Delay Sharp Roll-Off Filter Pass Band Ripple (1×/2×/4× Speed Mode)

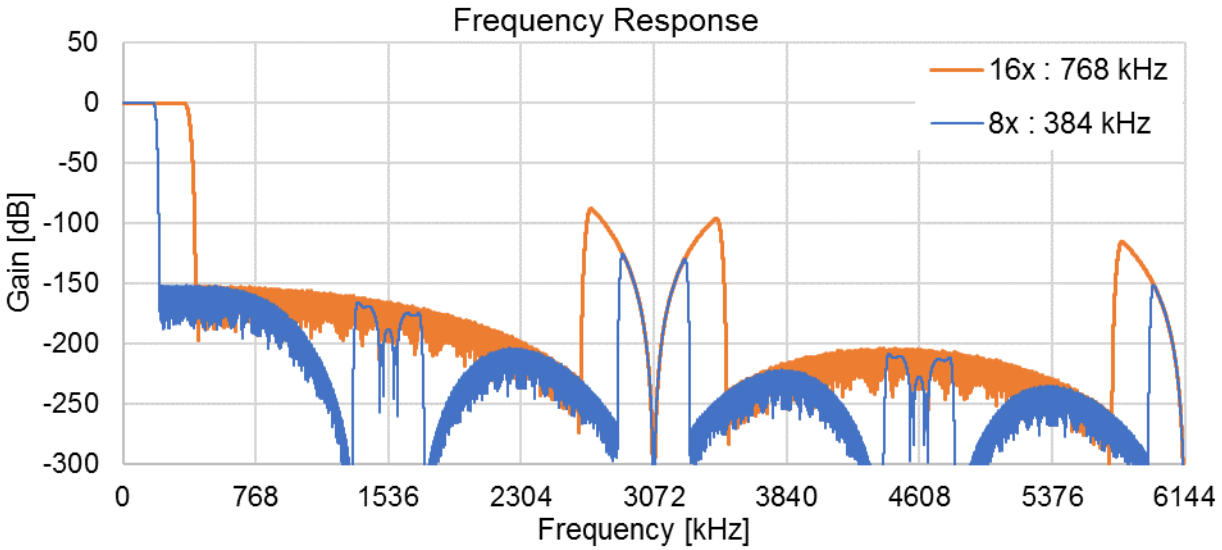


Figure 18. Short Delay Sharp Roll-Off Filter Frequency Response (8×/16× Speed Mode; to 6.144MHz)

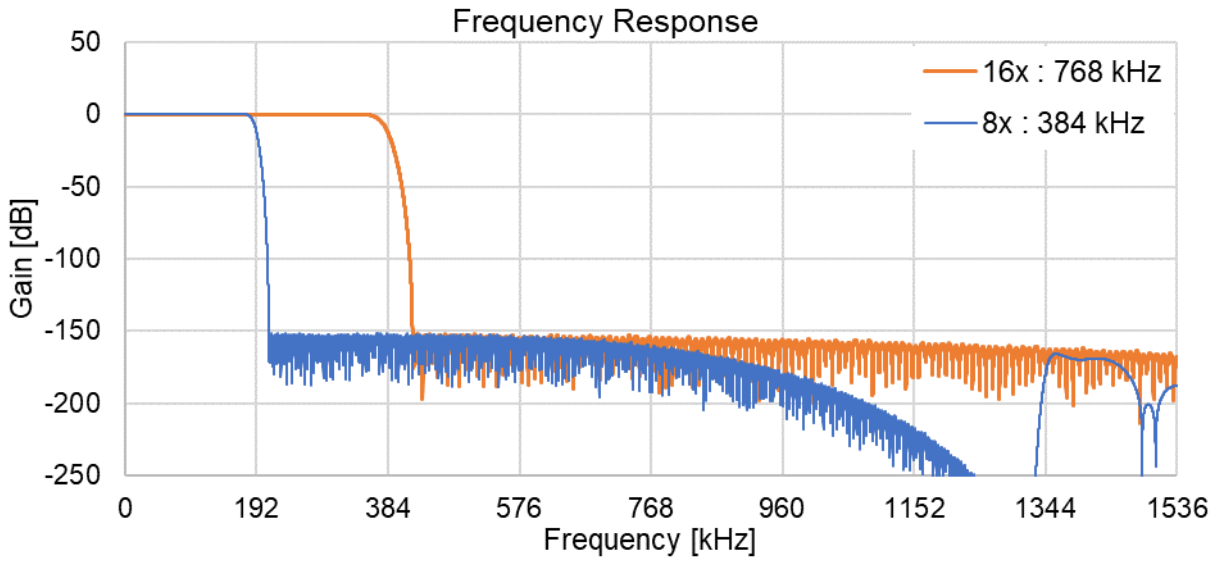


Figure 19. Short Delay Sharp Roll-Off Filter Frequency Response (8×/16× Speed Mode; to 1536kHz)

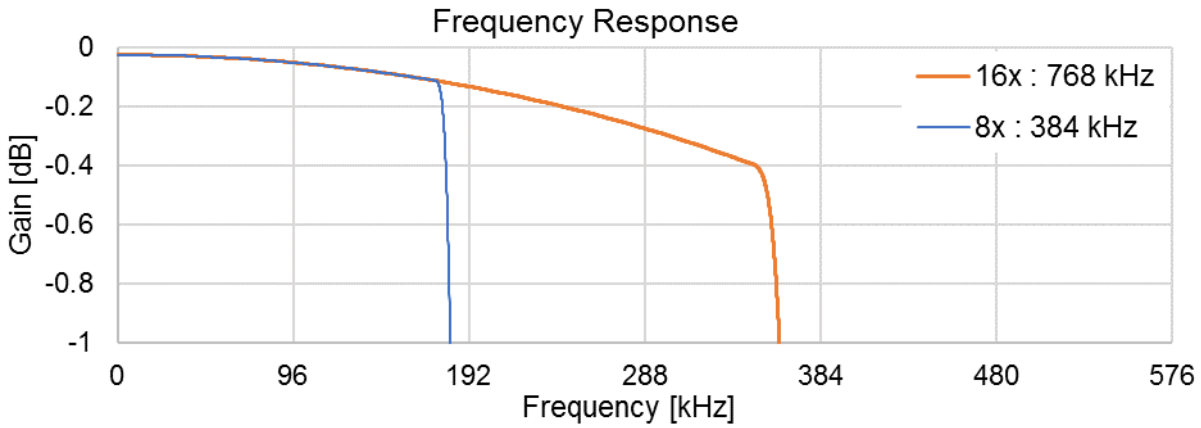


Figure 20. Short Delay Sharp Roll-Off Filter Pass Band Ripple (8×/16× Speed Mode)

8.2.4. Short Delay Slow Roll-Off Filter Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; DEM = OFF; SD bit = "1", SLOW bit = "1", SSLOW bit = "0"; unless otherwise specified)

▪ 1×/2×/4× Speed Mode (PCM mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.02 dB	-	0	-	0.1814fs	kHz
		–6.0 dB	-	-	0.4207fs	-	kHz
Pass band			PB	0	-	0.1814fs	kHz
Stop band			SB	0.8fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.01	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	1× Speed Mode		GD	-	5.4	-	1/fs
	2× Speed Mode		GD	-	5.4	-	1/fs
	4× Speed Mode		GD	-	5.1	-	1/fs

▪ 8×/16× Speed Mode (PCM and EXDF mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.1 dB	-	0	-	0.1836fs	kHz
		–6.0 dB	-	-	0.4195fs	-	kHz
Pass band			PB	0	-	0.1836s	kHz
Stop band			SB	0.888fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.01	dB
Stop band Attenuation		(Note 9)	SA	150	-	-	dB
Group Delay (Note 11)	8× Speed Mode		GD	-	7.2	-	1/fs
	16× Speed Mode		GD	-	6.1	-	1/fs

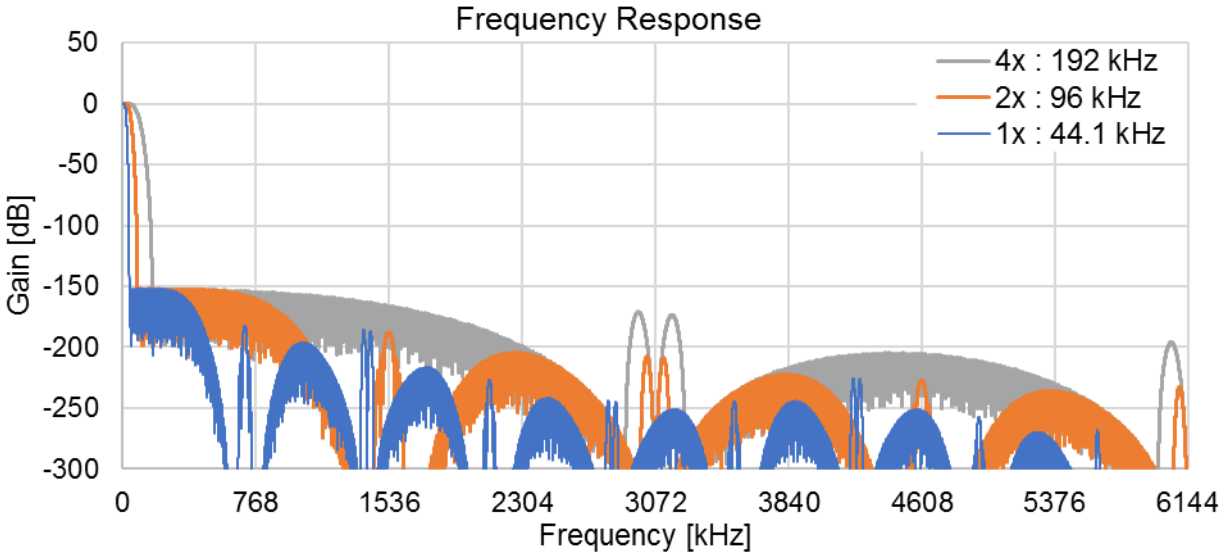


Figure 21. Short Delay Slow Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 6.144MHz)

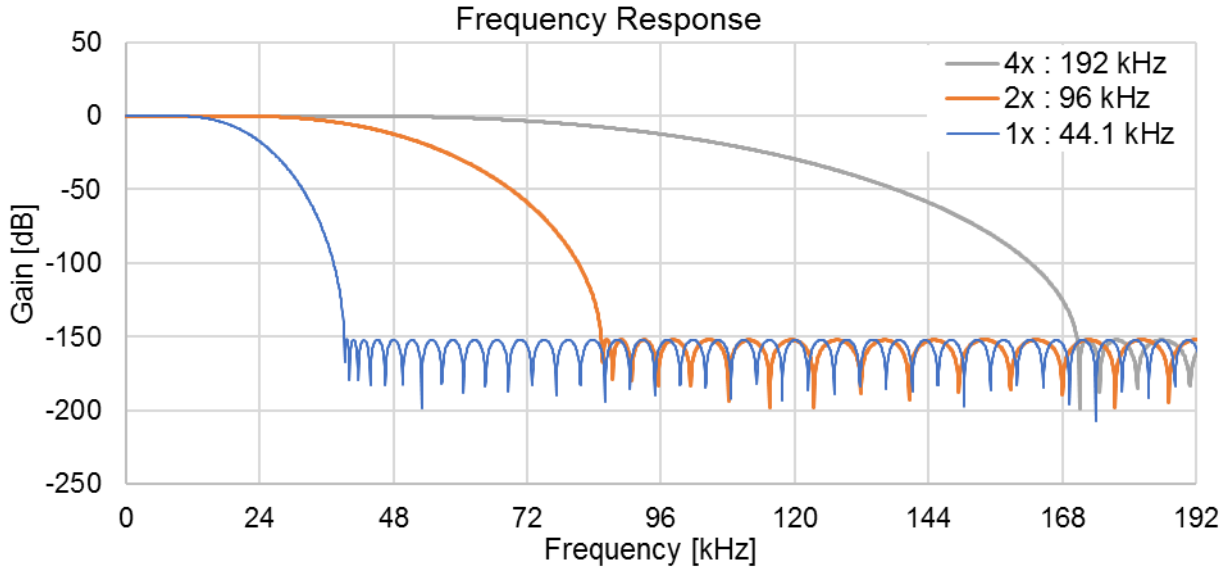


Figure 22. Short Delay Slow Roll-Off Filter Frequency Response (1×/2×/4× Speed Mode; to 192kHz)

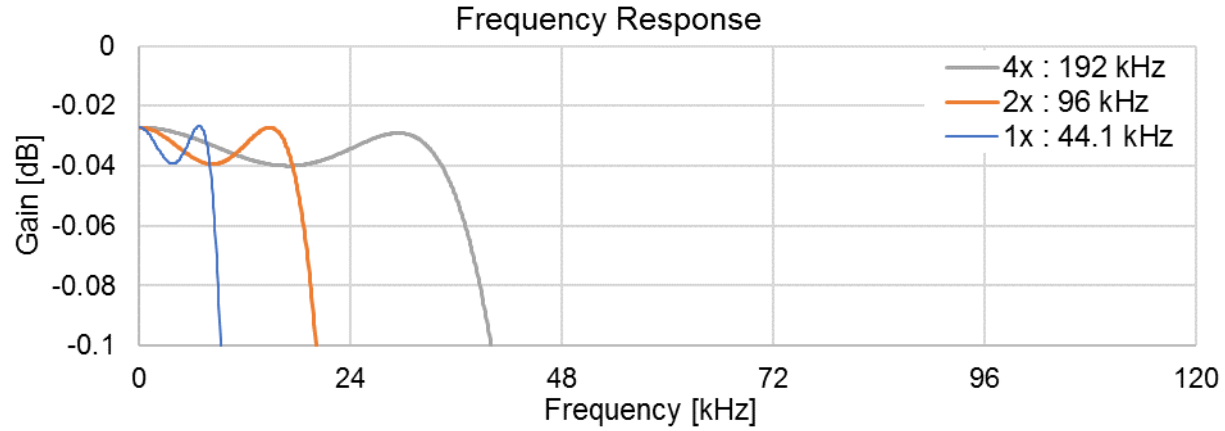


Figure 23. Short Delay Slow Roll-Off Filter Pass Band Ripple (1×/2×/4× Speed Mode)

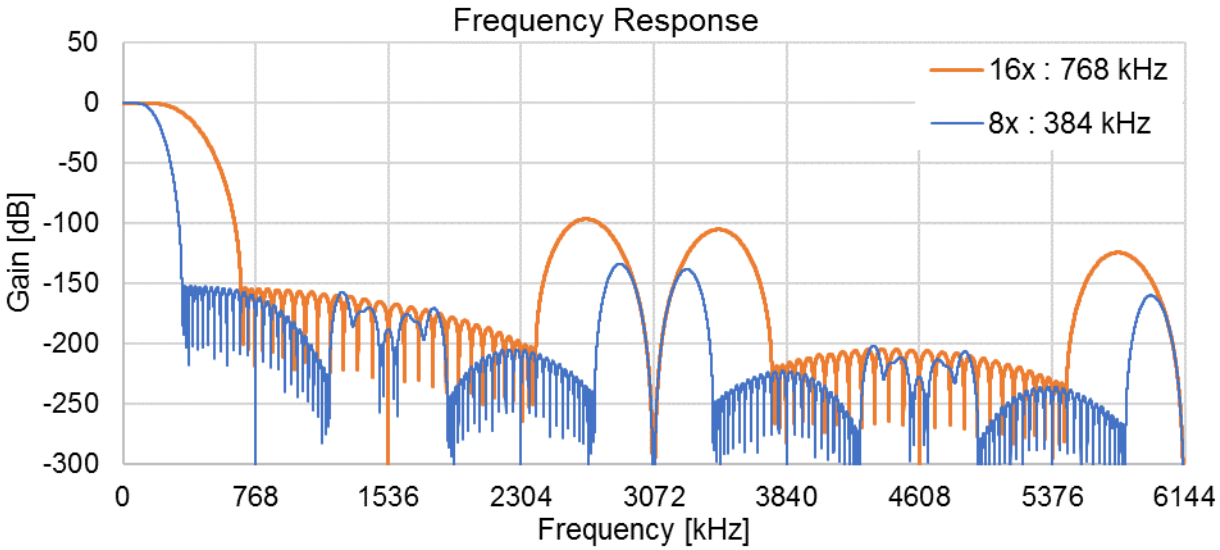


Figure 24. Short Delay Slow Roll-Off Filter Frequency Response
(8×/16× Speed Mode; to 6.144MHz)

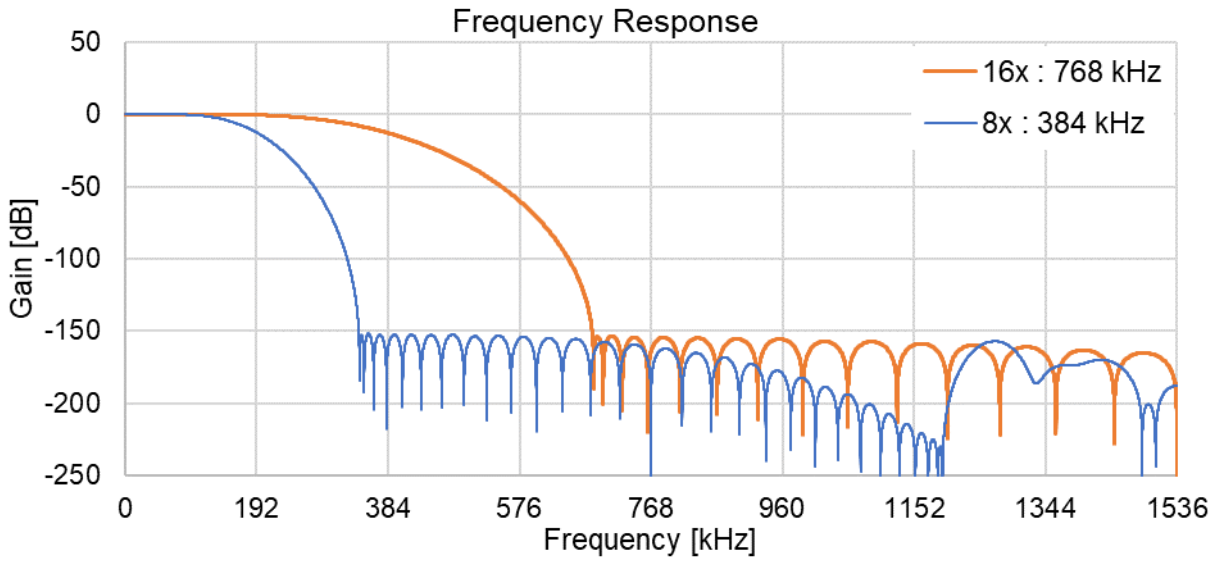


Figure 25. Short Delay Slow Roll-Off Filter Frequency Response (8×/16× Speed Mode; to 1536kHz)

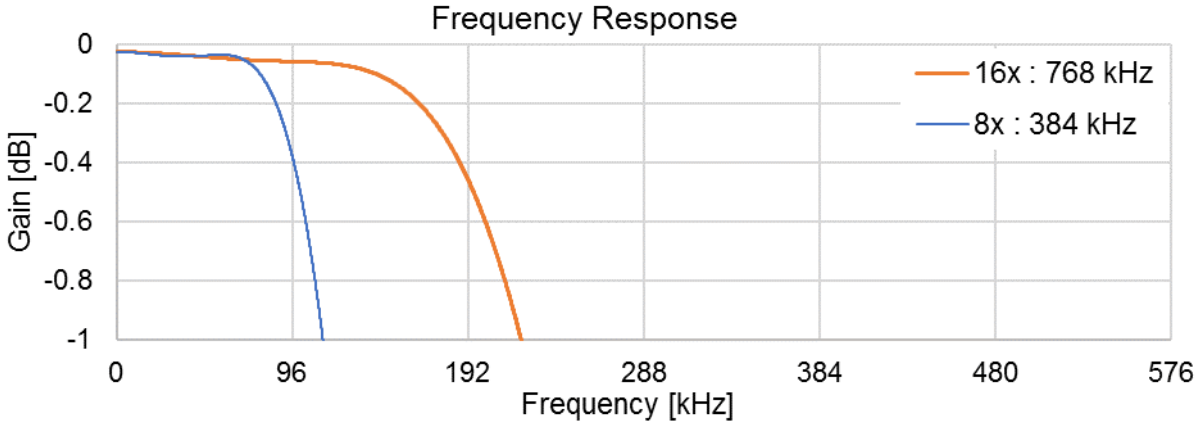


Figure 26. Short Delay Slow Roll-Off Filter Pass Band Ripple (8×/16× Speed Mode)

8.2.5. Low-dispersion Short Delay Filter Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; DEM = OFF; SD bit = "1", SLOW bit = "0", SSLOW bit = "1"; unless otherwise specified)

▪ 1×/2×/4× Speed Mode (PCM mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.02 dB	-	0	-	0.418fs	kHz
		–6.0 dB	-	-	0.5fs	-	kHz
Pass band			PB	0	-	0.418fs	kHz
Stop band			SB	0.582fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.01	dB
Stop band Attenuation		(Note 9)	SA	80	-	-	dB
Group Delay (Note 11)	1× Speed Mode		GD	-	10.5	-	1/fs
	2× Speed Mode		GD	-	10.5	-	1/fs
	4× Speed Mode		GD	-	10.3	-	1/fs
Group Delay Distortion			Δ GD	-	0.035	-	1/fs

▪ 8×/16× Speed Mode (PCM and EXDF mode)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)		–0.4 dB	-	0	-	0.418fs	kHz
		–6.0 dB	-	-	0.484fs	-	kHz
Pass band			PB	0	-	0.418fs	kHz
Stop band			SB	0.582fs	-	-	kHz
Pass band Ripple		(Note 10)	PR	-	-	±0.05	dB
Stop band Attenuation		(Note 9)	SA	80	-	-	dB
Group Delay (Note 11)	8× Speed Mode		GD	-	11.3	-	1/fs
	16× Speed Mode		GD	-	10.3	-	1/fs
Group Delay Distortion			Δ GD	-	0.035	-	1/fs

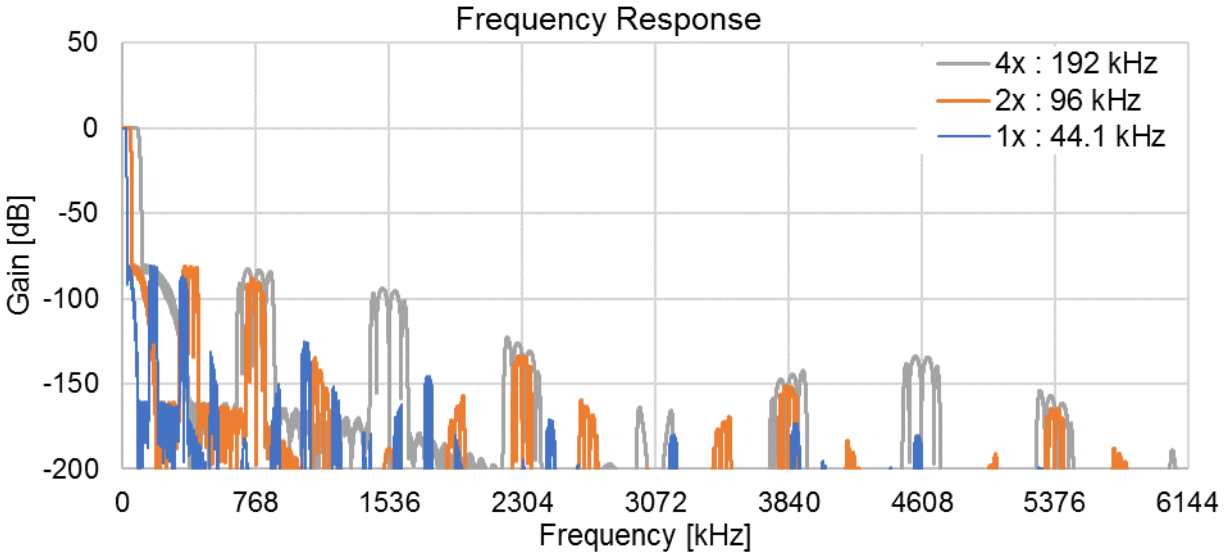


Figure 27. Low-dispersion Short Delay Filter Frequency Response
(1×/2×/4× Speed Mode; to 6.144MHz)

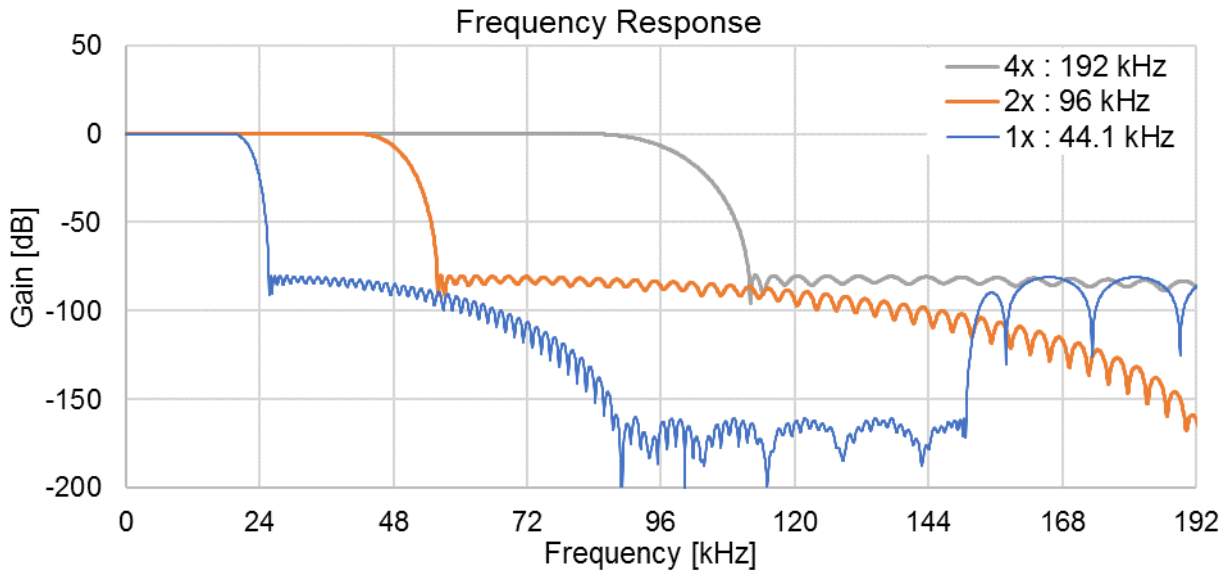


Figure 28. Low-dispersion Short Delay Filter Frequency Response (1×/2×/4× Speed Mode; to 192kHz)

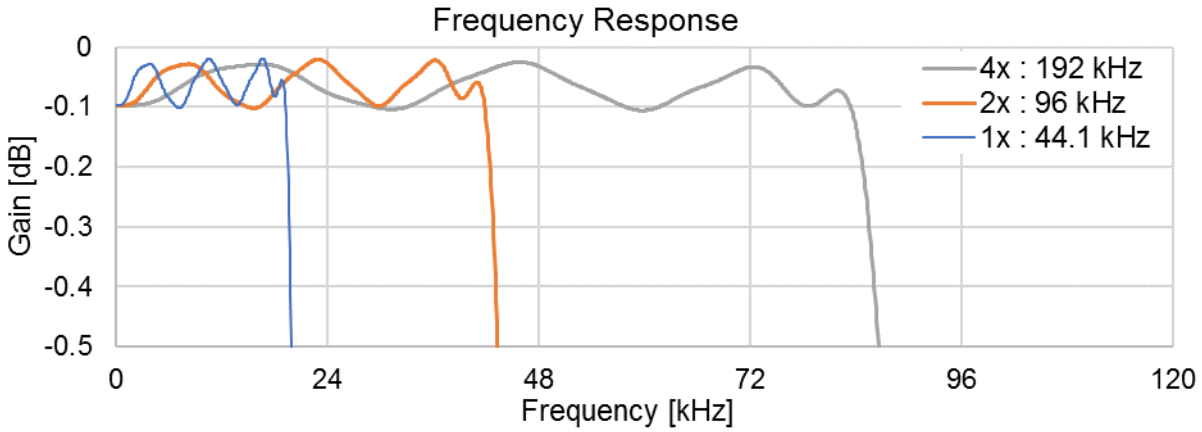


Figure 29. Low-dispersion Short Delay Filter Pass Band Ripple (1×/2×/4× Speed Mode)

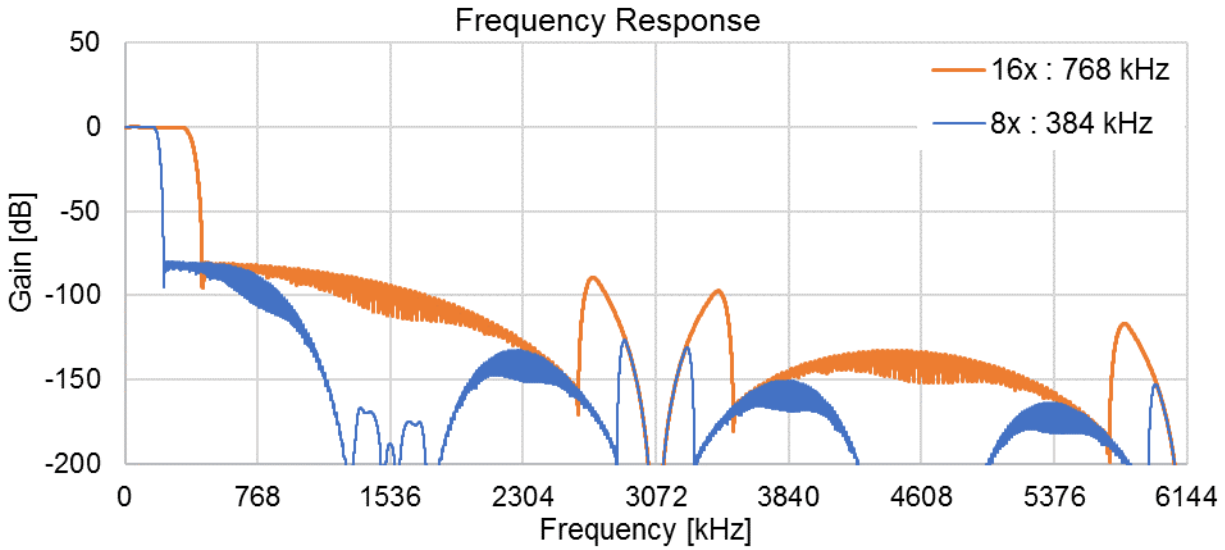


Figure 30. Low-dispersion Short Delay Filter Frequency Response (8×/16× Speed Mode; to 6.144MHz)

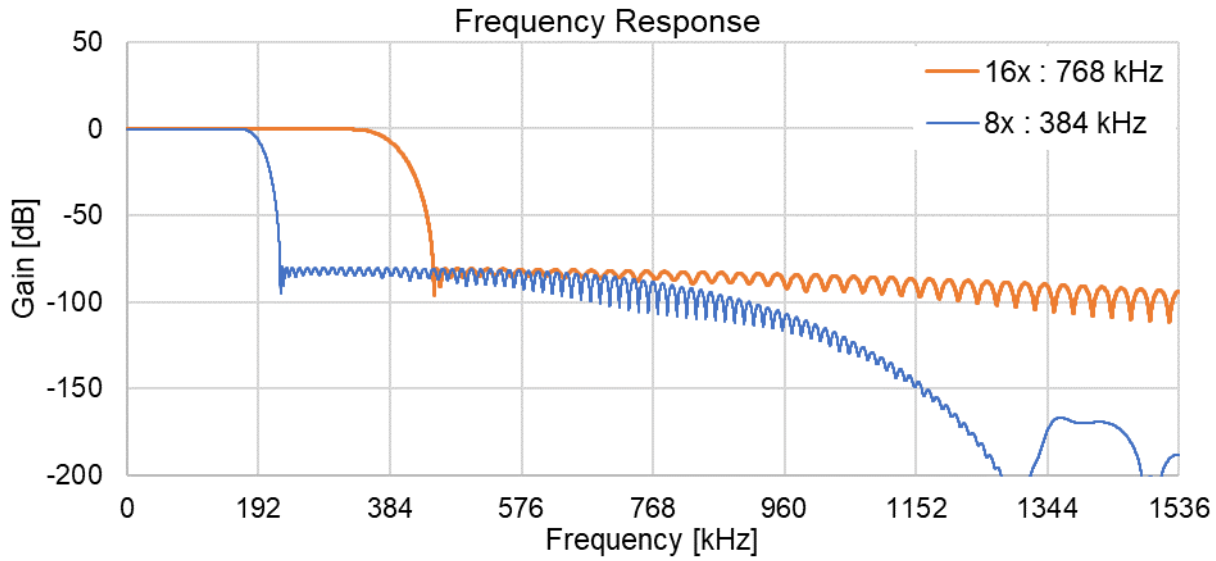


Figure 31. Low-dispersion Short Delay Filter Frequency Response (8×/16× Speed Mode; to 1536kHz)

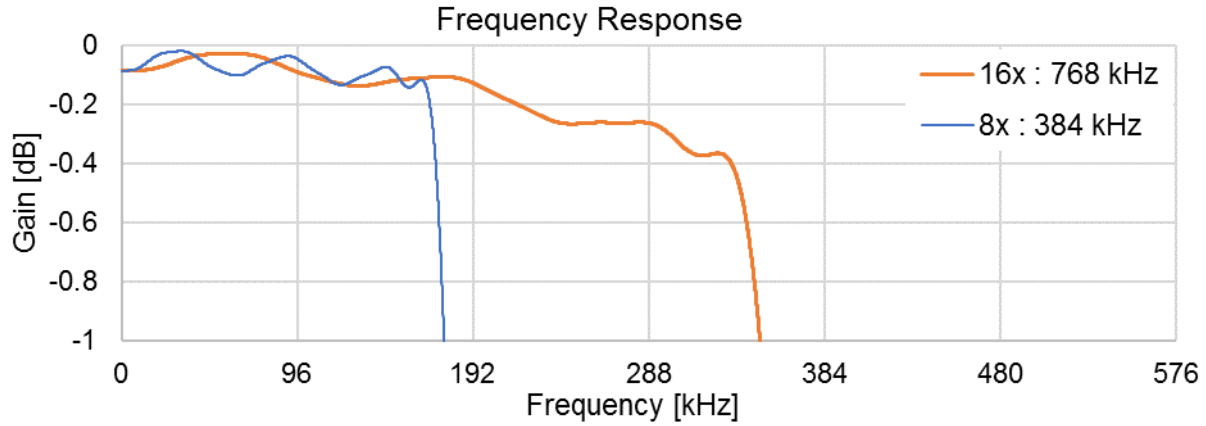


Figure 32. Low-dispersion Short Delay Filter Pass Band Ripple (8×/16× Speed Mode)

8.2.6. DSD Filter Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; unless otherwise specified)

8.2.6.1. DSD Normal Path (DSDD bit = "0")

(fsi = fDCLK)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	–0.02 dB	-	0	-	0.0067fsi	kHz
	–0.3 dB	-	-	0.0069fsi	-	kHz
	–3.0 dB	-	-	0.0079fsi	-	kHz
	–6.0 dB	-	-	0.0084fsi	-	kHz
	–10 dB	-	-	0.0089fsi	-	kHz
Pass band		PB	0	-	0.0067fsi	kHz
Stop band		SB	0.0111fsi	-	-	kHz
Pass band Ripple	(Note 10)	PR	-	-	±0.1	dB
Group Delay	(Note 11)	GD	-	390	-	1/fsi

Note 13. The output level is assumed as 0dB when a 1 kHz 25% to 75% duty sine wave is input. Pop noise may occur if the input signal exceeds 0dB.

8.2.6.2. DSD Volume Bypass (DSDD bit = “1”)
(1) DSDF bit = “0”

(fsi = fDCLK)

Parameter			Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	OBIT [1:0] = ”00” (DSD64/128)	−0.3 dB	-	0.0044fsi	-	kHz
		−3.0 dB	-	0.0132fsi	-	kHz
		−10.0 dB	-	0.0223fsi	-	kHz
	OBIT [1:0] = ”00” (DSD256/512)	−0.3 dB	-	0.0042fsi	-	kHz
		−3.0 dB	-	0.0128fsi	-	kHz
		−10.0 dB	-	0.0219fsi	-	kHz
	OBIT [1:0] = ”01” (DSD64/128/256/512)	−0.3 dB	-	0.0045fsi	-	kHz
		−3.0 dB	-	0.0137fsi	-	kHz
		−10.0 dB	-	0.0231fsi	-	kHz
	OBIT [1:0] = ”10”, ”11” (DSD64/128/256)	−0.3 dB	-	0.0044fsi	-	kHz
		−3.0 dB	-	0.0137fsi	-	kHz
		−10.0 dB	-	0.0233fsi	-	kHz

(2) DSDF bit = “1”

(fsi = fDCLK)

Parameter			Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	OBIT [1:0] = ”00” (DSD64/128)	−0.3 dB	-	0.0074fsi	-	kHz
		−3.0 dB	-	0.0231fsi	-	kHz
		−10.0 dB	-	0.0400fsi	-	kHz
	OBIT [1:0] = ”00” (DSD256/512)	−0.3 dB	-	0.0068fsi	-	kHz
		−3.0 dB	-	0.0210fsi	-	kHz
		−10.0 dB	-	0.0366fsi	-	kHz
	OBIT [1:0] = ”01” (DSD64/128/256/512)	−0.3 dB	-	0.0090fsi	-	kHz
		−3.0 dB	-	0.0273fsi	-	kHz
		−10.0 dB	-	0.0459fsi	-	kHz
	OBIT [1:0] = ”10”, ”11” (DSD64/128/256/512)	−0.3 dB	-	0.0090fsi	-	kHz
		−3.0 dB	-	0.0278fsi	-	kHz
		−10.0 dB	-	0.0462fsi	-	kHz

Note 14. The AK4191 does not support DSD1024 mode when DSDD bit =”1”.
As shown in Table 24, there are prohibited filter settings depending on OSR bit and OBIT [1:0] bits when DSDD bit =”1”.

8.2.7. Delta Sigma Modulator Data Input Filter Characteristics

(Ta = -40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; unless otherwise specified)

(fs = BCKI)

Parameter		Min.	Typ.	Max.	Unit
Frequency Response (Note 9)	–0.3 dB	-	0.0091fs	-	kHz
	–3.0 dB	-	0.0277fs	-	kHz
	–10.0 dB	-	0.0461fs	-	kHz

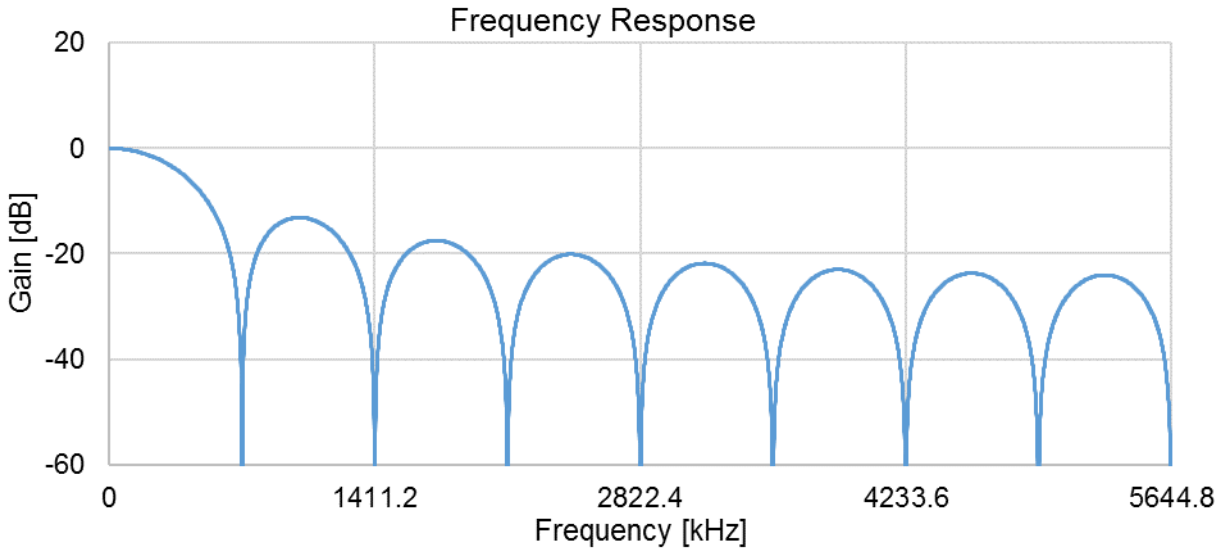


Figure 33. DATA MIX Filter Frequency Response

8.3. DC Characteristics

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V; unless otherwise specified.)
(TVDD× : TVDD1 or TVDD2 or TVDD3 or TVDD4. Please refer to 5.1 Pin Configurations)

Parameter	Symbol	Min.	Typ	Max.	Unit
Input Voltage					
Except SDA and SCL pin					
High-Level Input Voltage	VIH	80%TVDD×	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD×	V
SDA and SCL pin					
High-Level Input Voltage	VIH	70%TVDD1	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD1	V
Output Voltage					
Except SDA pin					
High-Level Output Voltage (Iout = –100 μA)	VOH	TVDD×–0.3	-	-	V
Low-Level Output Voltage (Iout = 100 μA)	VOL	-	-	0.3	V
SDA pin					
Low-Level Output Voltage					
2.0 V < TVDD1 ≦ 3.6 V (Iout = 3 mA)	VOL	-	-	0.4	V
1.7 V ≦ TVDD1 ≦ 2.0 V (Iout = 3 mA)	VOL	-	-	20%TVDD1	V
Pin Leak					
Input Leakage Current (Note 15)	Iin	-	-	±10	μA

Note 15. The TST1, TST2, BICK/BCK/DCLK, LRCK/DINR/DSDR and WCK pins have internal pull-down resistors. The resistance is 46 kΩ (typ) when TVDD1 = 3.3V. Therefore, these pins are not included in this specification.

8.4. Switching Characteristics

8.4.1. Audio Clocks in Synchronous Mode (DSYNCE bit = “0”)

(Ta = –40 to 85 °C; PVDD = 3.0 to 3.6 V, TVDD1 = 1.7 to 3.6 V, TVDD2 = 1.7 to 3.6 V, TVDD3 = 1.7 to 3.6 V, TVDD4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V, Cload = 20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (Note 16)						
Base MCLK Frequency	FS32K bit ="1"	fCLKb	7.68	-	8.704	MHz
	FS32K bit ="0"	fCLKb	10.752	-	13.824	MHz
MCLK Frequency		fCLK	-	2×fCLKb fCLKb 0.5×fCLKb 0.25×fCLKb	-	MHz
Duty Cycle		dCLK	40	-	60	%
LRCK Clock Timing (Slave Mode)						
Normal Mode (TDM [1:0] bits = “00”)						
1× speed mode	FS32K bit ="1"	fs	30	-	34	kHz
	FS32K bit ="0"	fs	42	-	54	kHz
2× speed mode		fs	87	-	108	kHz
4× speed mode		fs	174	-	216	kHz
8× speed mode		fs	348	-	388	kHz
16× speed mode		fs	696	-	776	kHz
32× Speed mode		fs	1392	-	1552	kHz
Duty Cycle		dfs	45	-	55	%
TDM128 Mode (TDM [1:0] bits = “01”)						
1× speed mode	FS32K bit ="1"	fs	30	-	34	kHz
	FS32K bit ="0"	fs	42	-	54	kHz
2× speed mode		fs	87	-	108	kHz
4× speed mode		fs	174	-	216	kHz
High time		tLRH	1/128fs	-	-	ns
Low time		tLRL	1/128fs	-	-	ns
TDM256 Mode (TDM [1:0] bits = “10”)						
1× speed mode	FS32K bit ="1"	fs	30	-	34	kHz
	FS32K bit ="0"	fs	42	-	54	kHz
2× speed mode		fs	87	-	108	kHz
High time		tLRH	1/256fs	-	-	ns
Low time		tLRL	1/256fs	-	-	ns
TDM512 Mode (TDM [1:0] bits = “11”)						
1× speed mode	FS32K bit ="1"	fs	30	-	34	kHz
	FS32K bit ="0"	fs	42	-	54	kHz
High time		tLRH	1/512fs	-	-	ns
Low time		tLRL	1/512fs	-	-	ns

Note 16. The MCLK frequency should be changed while the AK4191 is in reset state by setting the PDN pin = “L” or RSTN bit = “0”.

Parameter		Symbol	Min.	Typ.	Max.	Unit
BICK Clock and SDATA, SDATA2 Data Timing (Slave Mode)						
Normal Mode (TDM [1:0] bits = "00")						
BICK Period						
1× speed mode		tBCK	1/256fs	-	-	ns
2× speed mode		tBCK	1/128fs	-	-	ns
4× speed mode		tBCK	1/64fs	-	-	ns
8× speed mode		tBCK	1/64fs	-	-	ns
16× speed mode		tBCK	1/64fs	-	-	ns
32× Speed mode		tBCK	1/32fs	-	-	ns
BICK Pulse Width Low		tBCKL	9	-	-	ns
BICK Pulse Width High		tBCKH	9	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	5	-	-	ns
SDATA, SDATA2 Hold Time		tSDH	5	-	-	ns
SDATA, SDATA2 Setup Time		tSDS	5	-	-	ns
TDM128 Mode (TDM [1:0] bits = "01")						
BICK Period						
1× speed mode		tBCK	1/128fs	-	-	ns
2× speed mode		tBCK	1/128fs	-	-	ns
4× speed mode		tBCK	1/128fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM256 Mode (TDM [1:0] bits = "10")						
BICK Period						
1× speed mode		tBCK	1/256fs	-	-	ns
2× speed mode		tBCK	1/256fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM512 Mode (TDM [1:0] bits = "11")						
BICK Period						
1× speed mode		tBCK	1/512fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns

Note 17. It is defined so that LRCK edges do not occur at the same timing of a rising edge of BICK.

Parameter	Symbol	Min.	Typ.	Max.	Unit
LRCK Clock Timing (Master Mode) (Note 18)					
LRCK Output Frequency	fLRO	30	-	776	kHz
LRCK Output Duty Cycle	dLRO	-	50	-	%
BICK Output " ↓ " to LRCK Output Edge	tMBLR	-	±5	-	ns
BICK Clock Timing (Master Mode) (Note 18)					
BICK Output Frequency	fBICK	-	32/64/128 × fLRO	49664	kHz
BICK Output Duty Cycle	dBICKO	-	50	-	%
SDATA, SDATA2 Data Timing (Master Mode) (Note 18)					
SDATA, SDATA2 Hold Time	tSDH	5	-	-	ns
SDATA, SDATA2 Setup Time	tSDS	5	-	-	ns
EXDF Audio Interface Timing (Slave Mode)					
WCK Frequency					
×8 Over Sampling Mode	fWCK	348	-	388	kHz
×16 Over Sampling Mode	fWCK	696	-	776	kHz
×32 Over Sampling Mode	fWCK	1392	-	1552	kHz
WCK Edge to BCK "↑"	tWB	5	-	-	ns
WCK Pulse Width Low	tWCKL	2/fB	-	-	ns
WCK Pulse Width High	tWCKH	2/fB	-	-	ns
BCK Frequency					
×8 Over Sampling Mode	fB	-	32/48/64/96 × fWCK	-	kHz
×16 Over Sampling Mode	fB	-	32/48/64 × fWCK	-	kHz
×32 Over Sampling Mode	fB	-	32fWCK	-	kHz
BCK Pulse Width Low	tBL	9	-	-	ns
BCK Pulse Width High	tBH	9	-	-	ns
BCK "↑" to WCK Edge	tBW	5	-	-	ns
DINL/L2, DINR/R2 Hold Time	tDH	5	-	-	ns
DINL/L2, DINR/R2 Setup Time	tDS	5	-	-	ns
EXDF Audio Interface Timing (Master Mode) (Note 18)					
WCK Output Frequency	fWCKO	30	-	1552	kHz
WCK Output Duty Cycle	dWCKO	-	50	-	%
BCK Output " ↓ " to WCK Output Edge	tMBW	-	±5	-	ns
BCK Output Frequency	fBO		32 × fWCKO		
BCK Output Duty Cycle	dBO	-	50	-	%
DINL/L2, DINR/R2 Hold Time	tDH	5	-	-	ns
DINL/L2, DINR/R2 Setup Time	tDS	5	-	-	ns

Note 18. In Master mode (MSN bit = "1"), the AK4191 does not support asynchronous mode (DSYNCE = "1").

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD Audio Interface Timing (Slave Mode)					
Base Sampling Frequency FS32K bit ="0"	fsb	42	44.1	48.5	kHz
(DSD64 Mode, DSDSEL [2:0] bits = "000")					
DCLK Period	tDCK	-	1/64fsb	-	ns
DCLK Pulse Width Low	tDCKL	144	-	-	ns
DCLK Pulse Width High	tDCKH	144	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	–20	-	20	ns
(DSD128 Mode, DSDSEL [2:0] bits = "001")					
DCLK Period	tDCK	-	1/128fsb	-	ns
DCLK Pulse Width Low	tDCKL	72	-	-	ns
DCLK Pulse Width High	tDCKH	72	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	–10	-	10	ns
(DSD256 Mode, DSDSEL [2:0] bits = "010")					
DCLK Period	tDCK	-	1/256fsb	-	ns
DCLK Pulse Width Low	tDCKL	36	-	-	ns
DCLK Pulse Width High	tDCKH	36	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	–5	-	5	ns
(DSD512 Mode, DSDSEL [2:0] bits = "011")					
DCLK Period	tDCK	-	1/512fsb	-	ns
DCLK Pulse Width Low	tDCKL	18	-	-	ns
DCLK Pulse Width High	tDCKH	18	-	-	ns
DSDL/R Setup Time	tDDS	5	-	-	ns
DSDL/R Hold Time	tDDH	5	-	-	ns
(DSD1024 Mode, DSDSEL [2:0] bits = "100")					
DCLK Period	tDCK	-	1/1024fsb	-	ns
DCLK Pulse Width Low	tDCKL	9		-	ns
DCLK Pulse Width High	tDCKH	9		-	ns
DSDL/R Setup Time	tDDS	4		-	ns
DSDL/R Hold Time	tDDH	4		-	ns

Note 19. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio data format is in phase modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

8.4.2. Audio Clocks in Asynchronous Mode (DSYNCE bit = "1")

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (Note 16)					
Base MCLK Frequency					
Base Sampling Frequency = 44.1 kHz	fCLKb	11.18	11.2896	11.40	MHz
Base Sampling Frequency = 48 kHz	fCLKb	12.17	12.288	12.41	MHz
MCLK Frequency	fCLK	-	fCLKb×2 fCLKb fCLKb/2 fCLKb/4	-	MHz
Duty Cycle	dCLK	40	-	60	%
LRCK Clock Timing (Slave Mode)					
Base Sampling Frequency	fsb	43.7	44.1	44.5	kHz
	fsb	47.6	48	48.4	kHz
Normal Mode (TDM [1:0] bits = "00")					
1× speed mode	fs	-	fsb	-	kHz
2× speed mode	fs	-	2fsb	-	kHz
4× speed mode	fs	-	4fsb	-	kHz
8× speed mode	fs	-	8fsb	-	kHz
16× speed mode	fs	-	16fsb	-	kHz
32× Speed mode	fs	-	32fsb	-	kHz
Duty Cycle	dfs	45	-	55	%
TDM128 Mode (TDM [1:0] bits = "01")					
1× speed mode	fs	-	fsb	-	kHz
2× speed mode	fs	-	2fsb	-	kHz
4× speed mode	fs	-	4fsb	-	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 Mode (TDM [1:0] bits = "10")					
1× speed mode	fs	-	fsb	-	kHz
2× speed mode	fs	-	2fsb	-	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 Mode (TDM [1:0] bits = "11")					
1× speed mode	fs	-	fsb	-	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns

Parameter		Symbol	Min.	Typ.	Max.	Unit
BICK Clock and SDATA, SDATA2 Data Timing (Slave Mode)						
Normal Mode (TDM [1:0] bits = "00")						
BICK Period						
1× speed mode		tBCK	1/256fs	-	-	ns
2× speed mode		tBCK	1/128fs	-	-	ns
4× speed mode		tBCK	1/64fs	-	-	ns
8× speed mode		tBCK	1/64fs	-	-	ns
16× speed mode		tBCK	1/64fs	-	-	ns
32× Speed mode		tBCK	1/32fs	-	-	ns
BICK Pulse Width Low		tBCKL	9	-	-	ns
BICK Pulse Width High		tBCKH	9	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	5	-	-	ns
SDATA, SDATA2 Hold Time		tSDH	5	-	-	ns
SDATA, SDATA2 Setup Time		tSDS	5	-	-	ns
TDM128 Mode (TDM [1:0] bits = "01")						
BICK Period						
1× speed mode		tBCK	1/128fs	-	-	ns
2× speed mode		tBCK	1/128fs	-	-	ns
4× speed mode		tBCK	1/128fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM256 Mode (TDM [1:0] bits = "10")						
BICK Period						
1× speed mode		tBCK	1/256fs	-	-	ns
2× speed mode		tBCK	1/256fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM512 Mode (TDM [1:0] bits = "11")						
BICK Period						
1× speed mode		tBCK	1/512fs	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
EXDF Audio Interface Timing (Slave Mode)					
Base Sampling Frequency	fsb	43.7	44.1	44.5	kHz
	fsb	47.6	48	48.4	kHz
WCK Frequency					
×8 Over Sampling Mode	fWCK	-	8fsb	-	kHz
×16 Over Sampling Mode	fWCK	-	16fsb	-	kHz
×32 Over Sampling Mode	fWCK	-	32fsb	-	kHz
WCK Edge to BCK "↑"	tWB	5	-	-	ns
WCK Pulse Width Low	tWCKL	2/fB	-	-	ns
WCK Pulse Width High	tWCKH	2/fB	-	-	ns
BCK Frequency					
×8 Over Sampling Mode	fB	-	32/48/64/96 × fWCK	-	kHz
×6 Over Sampling Mode	fB	-	32/48/64 × fWCK	-	kHz
×32 Over Sampling Mode	fB	-	32fWCK	-	kHz
BCK Pulse Width Low	tBL	9	-	-	ns
BCK Pulse Width High	tBH	9	-	-	ns
BCK "↑" to WCK Edge	tBW	5	-	-	ns
DINL/L2, DINR/R2 Hold Time	tDH	5	-	-	ns
DINL/L2, DINR/R2 Setup Time	tDS	5	-	-	ns
DSD Audio Interface Timing (Slave Mode)					
Base Sampling Frequency	fsb	43.7	44.1	44.5	kHz
	fsb	47.6	48	48.4	kHz
(DSD64 Mode, DSDSEL [2:0] bits = "000")					
DCLK Period	tDCK	-	1/64fsb	-	ns
DCLK Pulse Width Low	tDCKL	144	-	-	ns
DCLK Pulse Width High	tDCKH	144	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−20	-	20	ns
(DSD128 Mode, DSDSEL [2:0] bits = "001")					
DCLK Period	tDCK	-	1/128fsb	-	ns
DCLK Pulse Width Low	tDCKL	72	-	-	ns
DCLK Pulse Width High	tDCKH	72	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−10	-	10	ns
(DSD256 Mode, DSDSEL [2:0] bits = "010")					
DCLK Period	tDCK	-	1/256fsb	-	ns
DCLK Pulse Width Low	tDCKL	36	-	-	ns
DCLK Pulse Width High	tDCKH	36	-	-	ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−5	-	5	ns
(DSD512 Mode, DSDSEL [2:0] bits = "011")					
DCLK Period	tDCK	-	1/512fsb	-	ns
DCLK Pulse Width Low	tDCKL	18	-	-	ns
DCLK Pulse Width High	tDCKH	18	-	-	ns
DSDL/R Setup Time	tDDS	5	-	-	ns
DSDL/R Hold Time	tDDH	5	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
(DSD1024 Mode, DSDSEL [2:0] bits = "100")					
DCLK Period	tDCK	-	1/1024fsb	-	ns
DCLK Pulse Width Low	tDCKL	9		-	ns
DCLK Pulse Width High	tDCKH	9		-	ns
DSDL/R Setup Time	tDDS	4		-	ns
DSDL/R Hold Time	tDDH	4		-	ns

8.4.3. Multi-Bit Audio-IF Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Delta Sigma Modulator Data Output Interface Timing					
BCKO Clock Timing					
256fs Mode (OSR bit = "0")					
BCKO Period	tBCKO	-	1/fCLKb	-	ns
128fs Mode (OSR bit = "1")					
BCKO Period	tBCKO	-	2/fCLKb	-	ns
Duty Cycle	dBCKO		50		%
MBD7-1 Output Data Timing					
MONO mode (OSTME bit = "0")					
BCK fall Edge to MBD7-1	tMBDD	-	±5	-	ns
STEREO mode (OSTME bit = "1")					
BCK Edge to MBD7-1	tMBDD	-	±5	-	ns
Delta Sigma Modulator Data Input Interface Timing					
BCKI Clock Timing (Slave Mode)					
256fs Mode (DSMIFS bit = "0")					
BCKI Period	tBCKI	-	1/fCLKb	-	ns
128fs Mode (DSMIFS bit = "1")					
BCKI Period	tBCKI	-	2/fCLKb	-	ns
Duty Cycle	dBCKI	45		55	%
DSMI1-7 Input Data Timing (Slave Mode)					
MONO mode (ISTME bit = "0")					
DSMI7-1 Hold Time	tDSMH	4	-	-	ns
DSMI7-1 Setup Time	tDSMS	4	-	-	ns
STEREO mode (ISTME bit = "1")					
BCK Edge to DSMI7-1	tDSMD	–5	-	5	ns

8.4.4. Control Interface and Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (4-wire Serial Control Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
CCLK "↓" to CDTO Edge	tDCD	-	-	45	ns
CSN " ↑ " to CDTO "Hi-Z"	tCCZ	-	-	70	ns
PROG Edge to CSN "↓"	tPCS	10	-	-	us
CSN "↑" to PROG Edge	tCSP	10	-	-	us
Control Interface Timing (I^2C-Bus Control Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width	tAPD	600	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

8.5. Timing Diagram

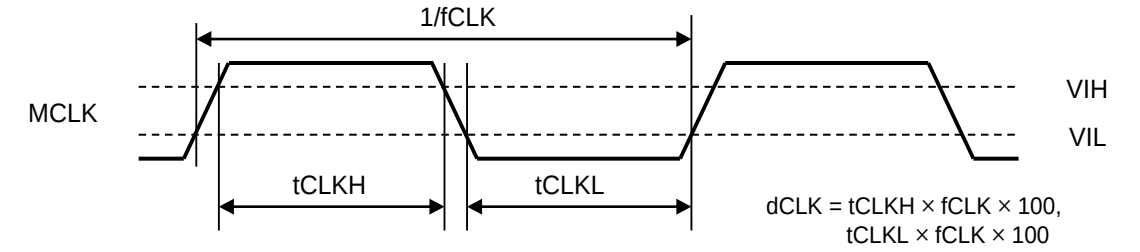


Figure 34. Master Clock Timing

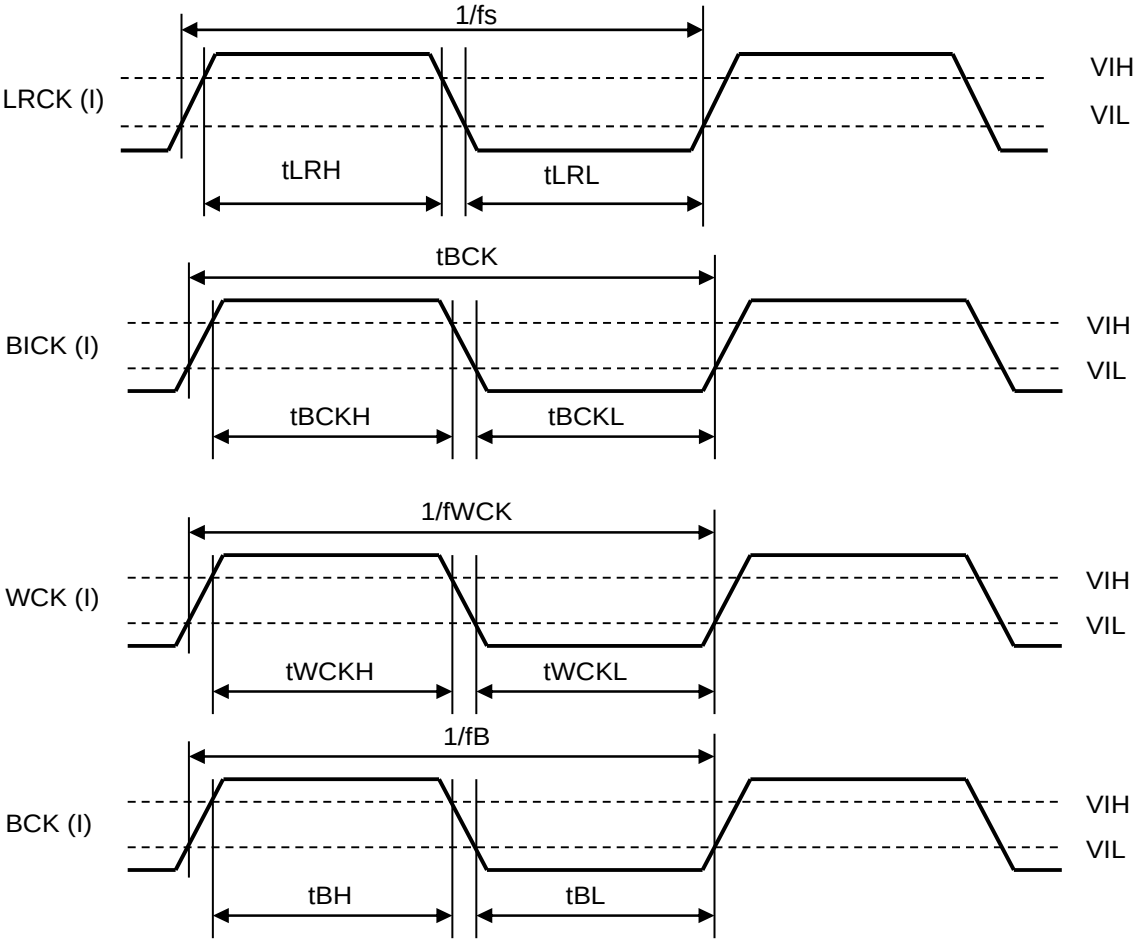


Figure 35. Audio Clock Timing (Slave Mode)

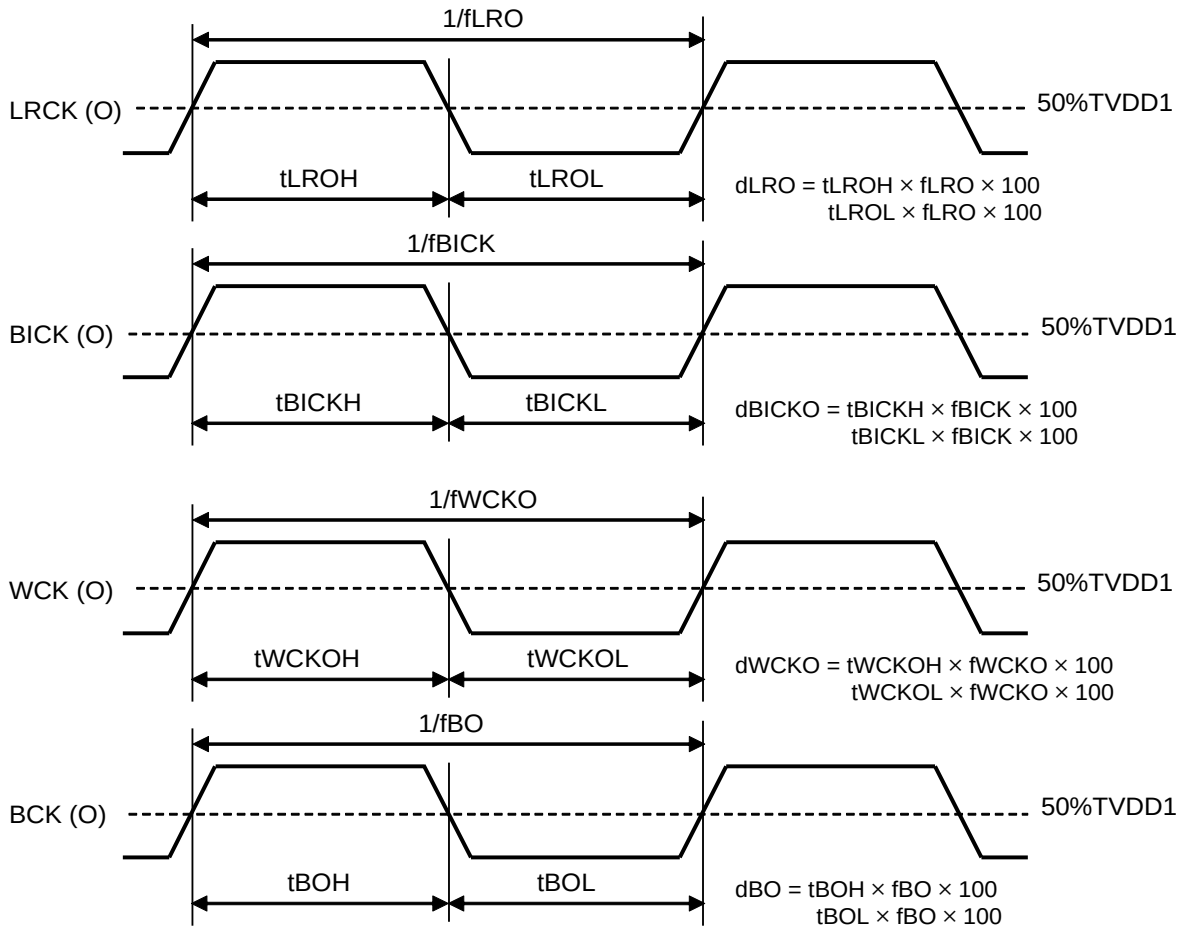


Figure 36. Audio Clock Timing (Master Mode)

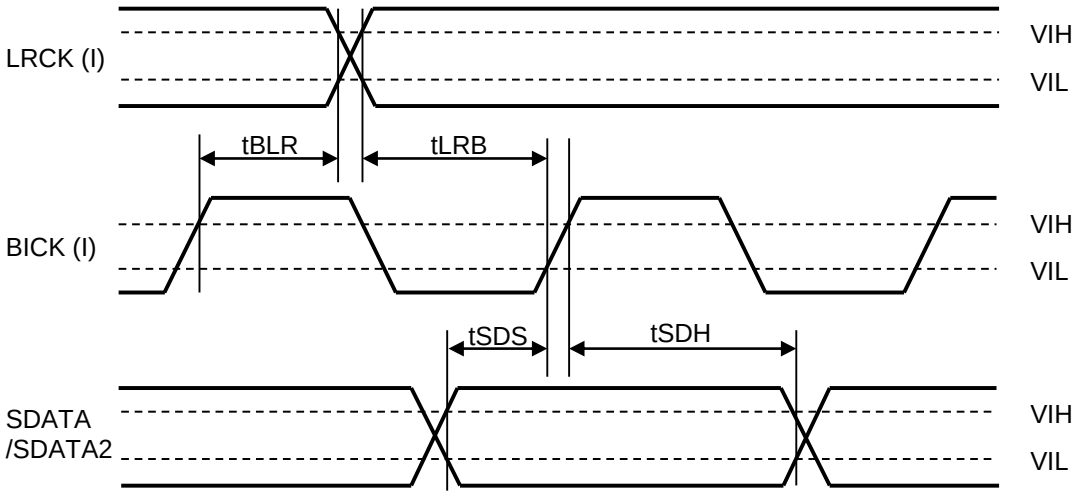


Figure 37. Audio Interface Timing (PCM：Slave Mode)

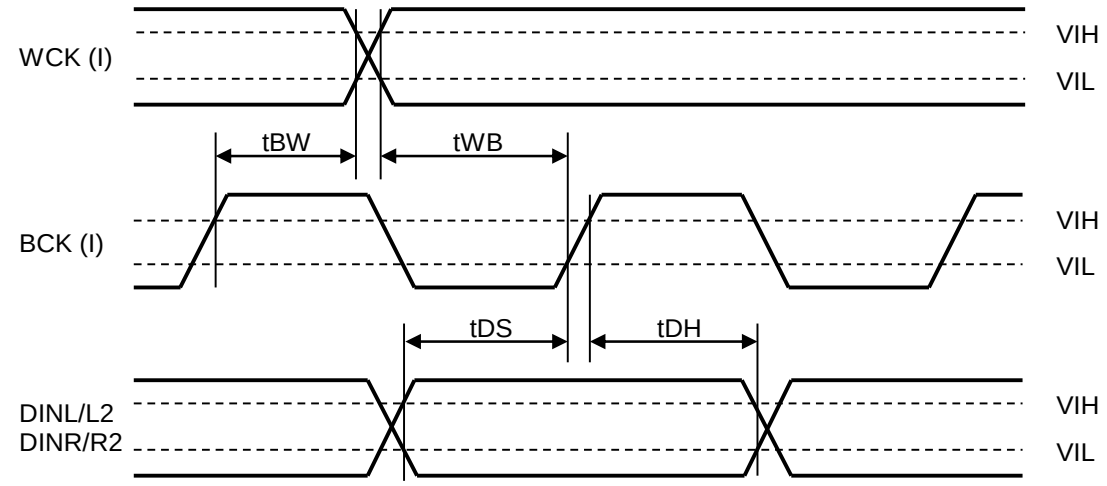


Figure 38. Audio Interface Timing (External Digital Filter I/F：Slave Mode)

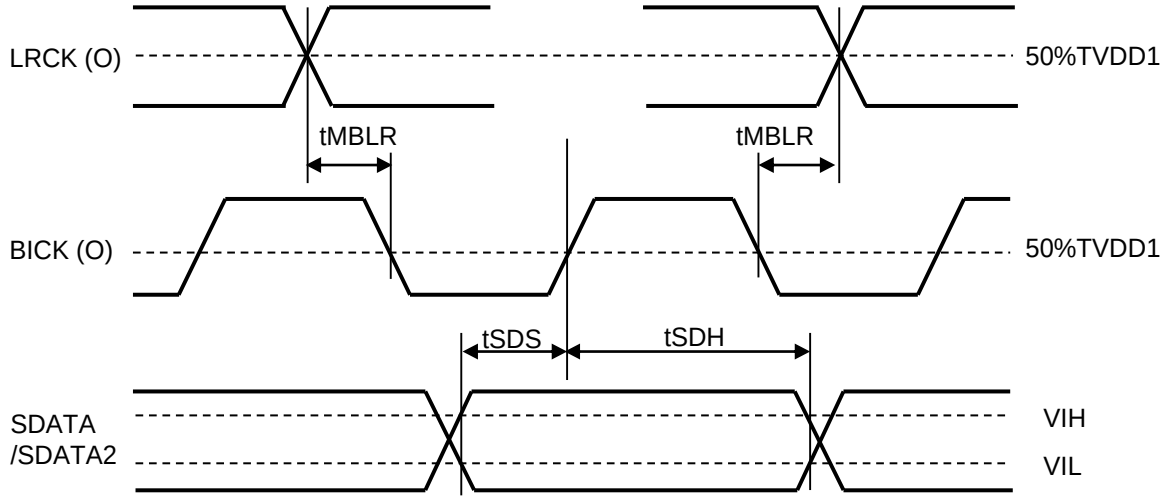


Figure 39. Audio Interface Timing (PCM：Master Mode)

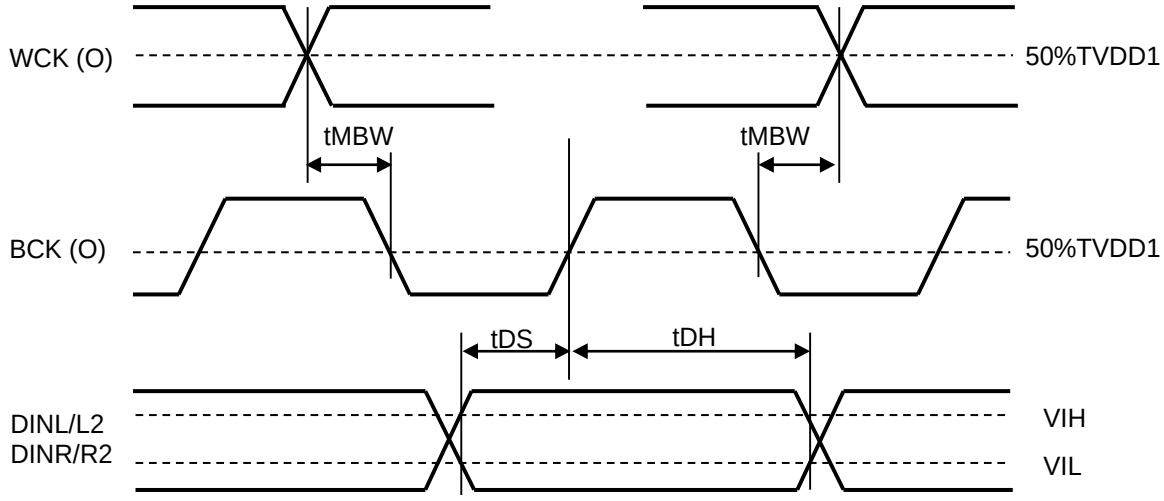


Figure 40. Audio Interface Timing (External Digital Filter I/F：Master Mode)

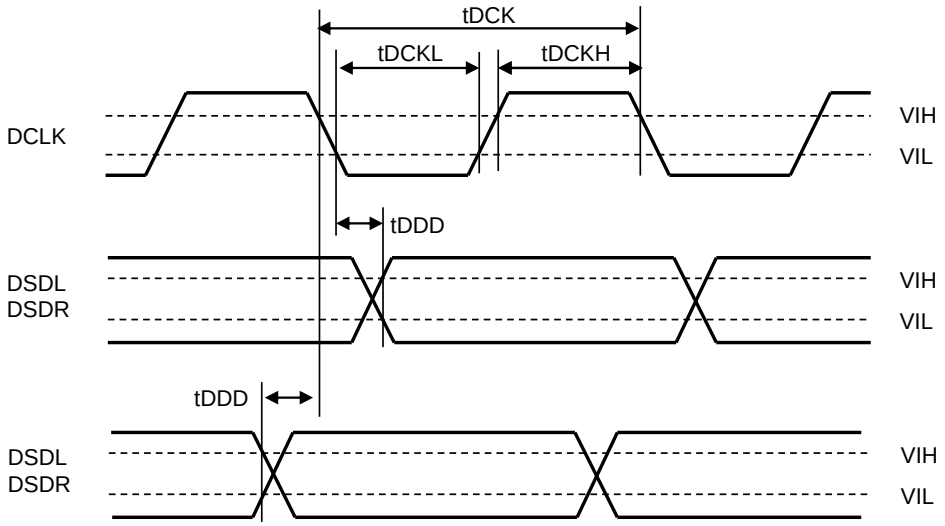
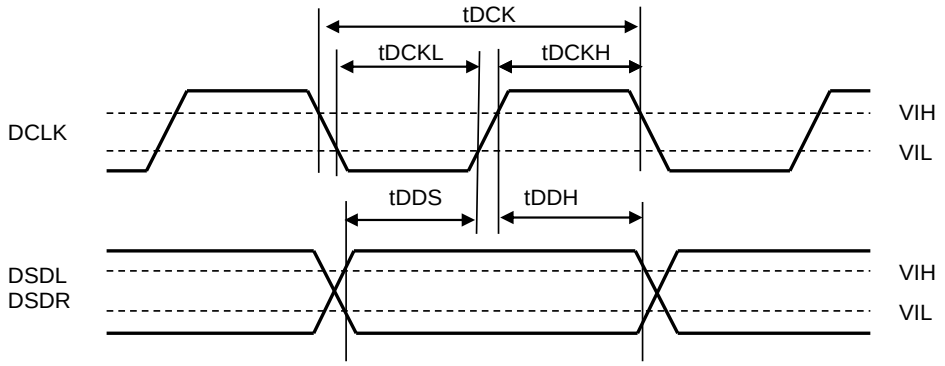


Figure 41. DSD Audio Interface Timing (DSD64/128/256 Mode)



DSD Audio Interface Timing (DSD512/1024 Mode)

Figure 42. Audio Interface Timing (DSD Mode, DCKB bit = “0”)

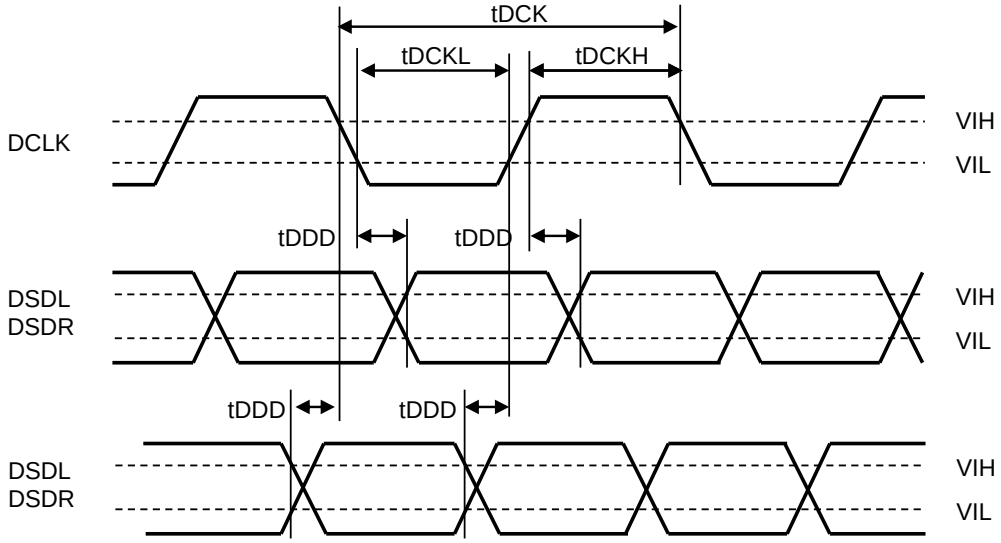


Figure 43. Audio Interface Timing (DSD Mode, Phase Modulation Format, DCKB bit = “0”)

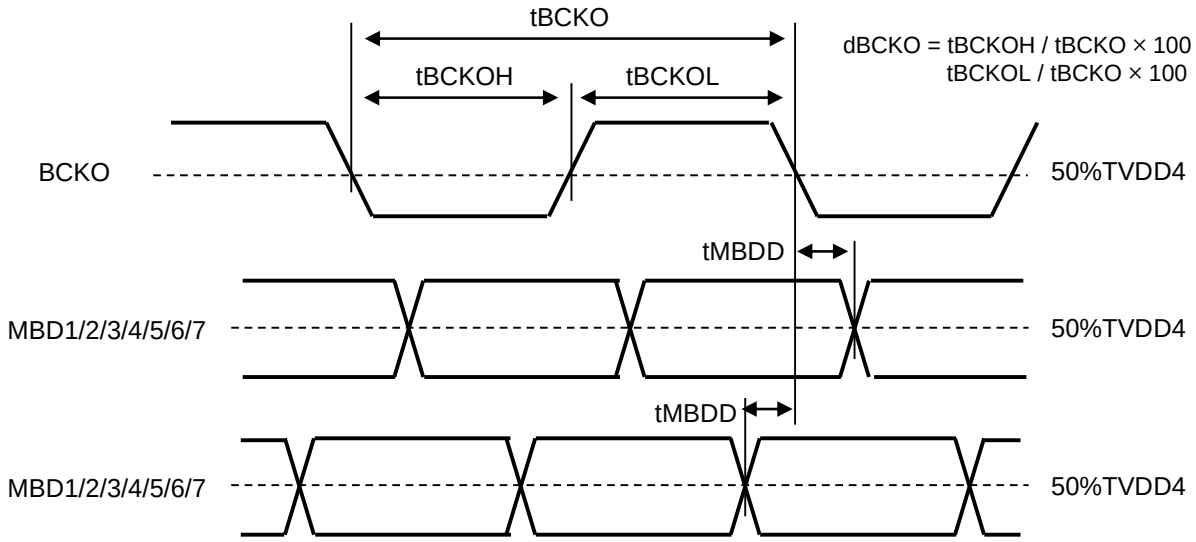


Figure 44. Delta Sigma Modulator Data Output Interface Timing (OSTME bit = ”0”)

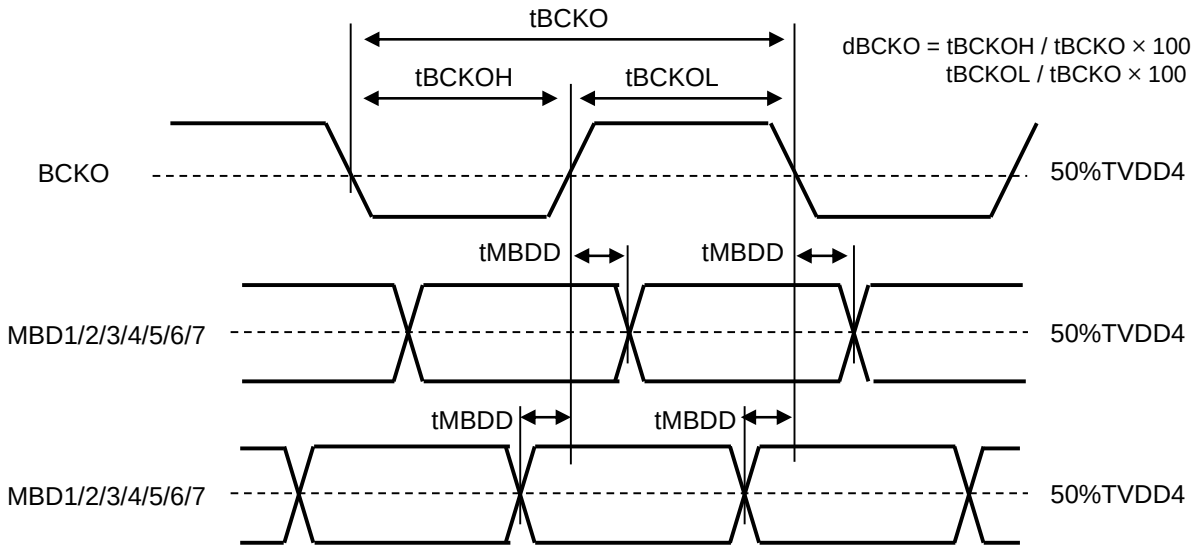


Figure 45. Delta Sigma Modulator Data Output Interface Timing (OSTME bit = ”1”)

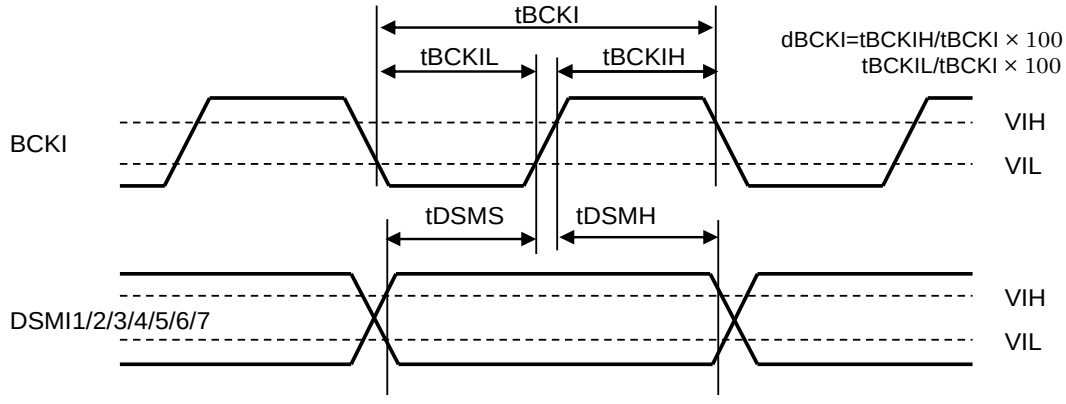


Figure 46. Delta Sigma Modulator Data Input Interface Timing (ISTME bit = ”0”)

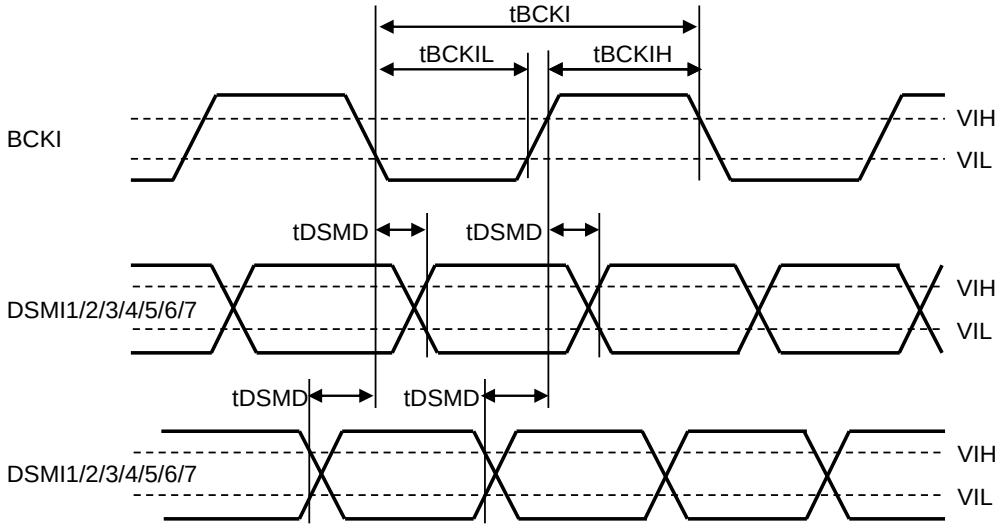


Figure 47. Delta Sigma Modulator Data Interface Input Timing (ISTME bit = ”1”)

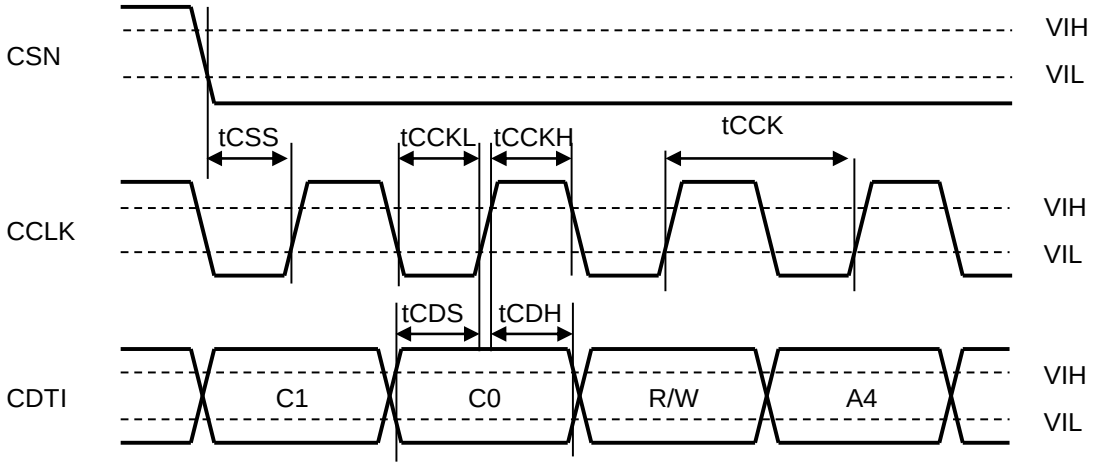


Figure 48. WRITE Command Input Timing (4-wire Serial Control Mode)

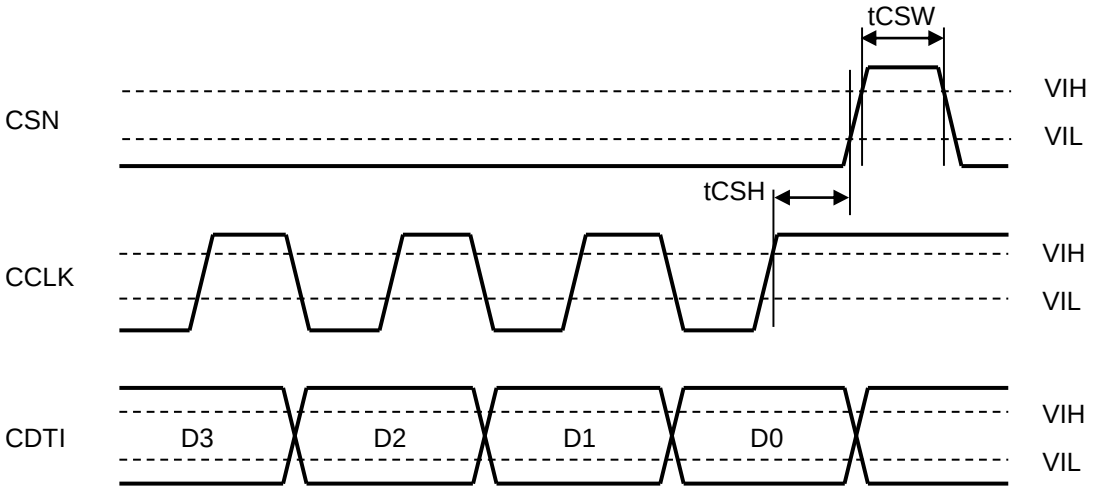


Figure 49. WRITE Data Input Timing (4-wire Serial Control Mode)

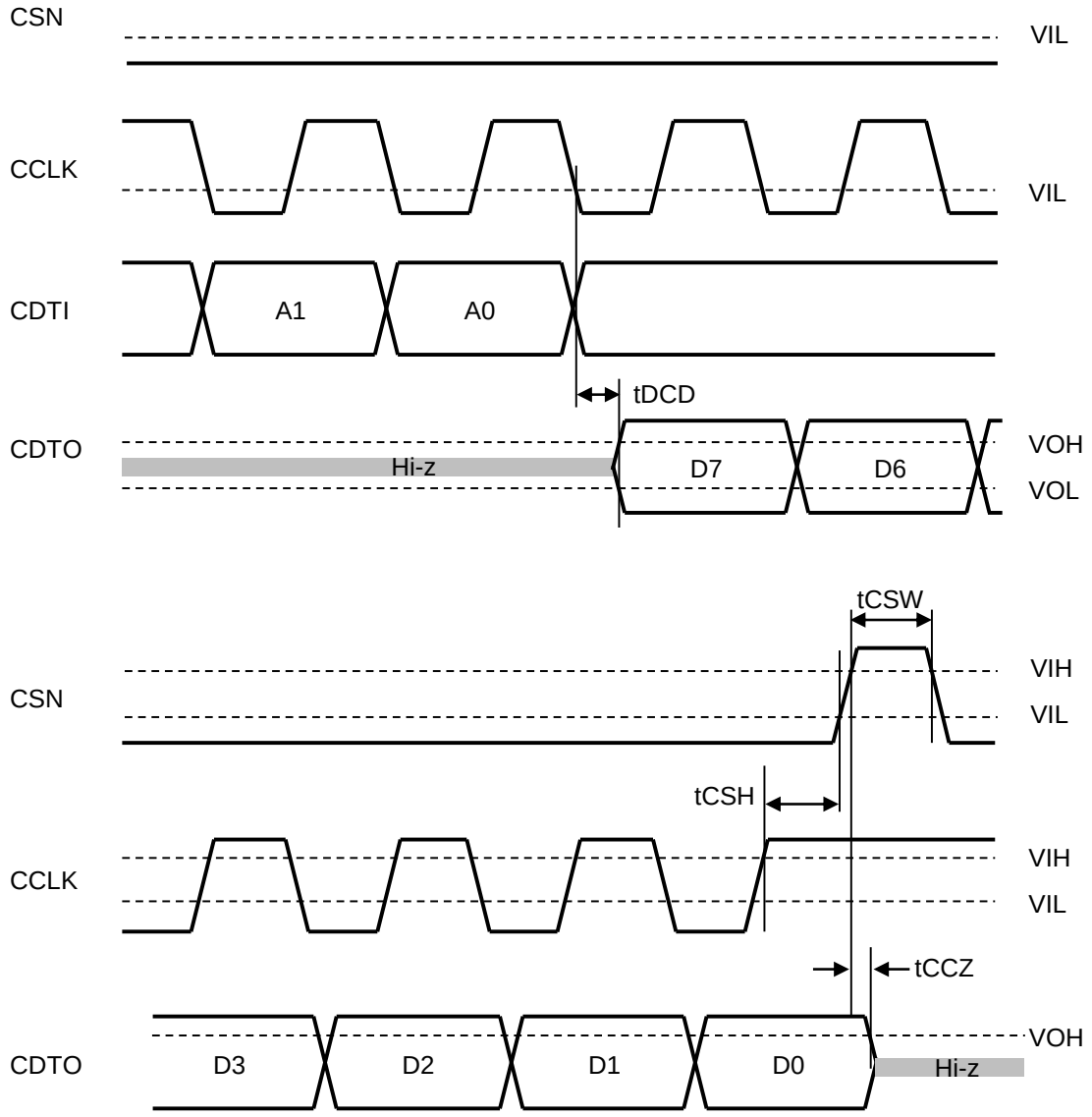


Figure 50. READ Data Output Timing (4-wire Serial Control Mode)

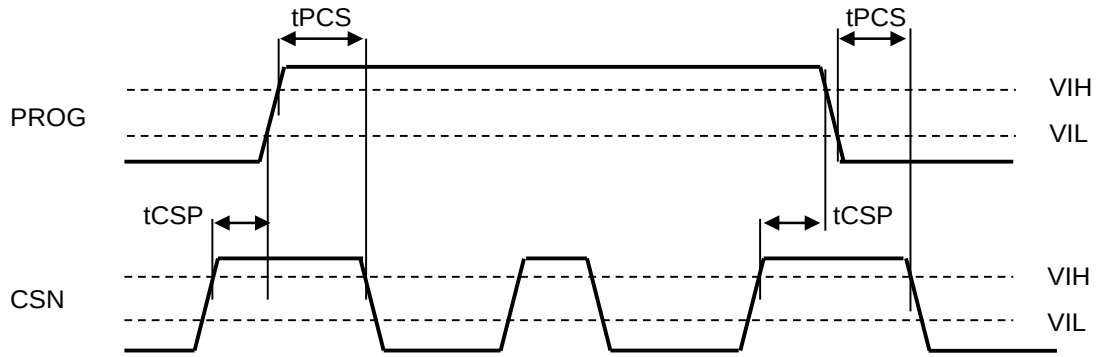


Figure 51. PROG and CSN Input Timing (4-wire Serial Control Mode)

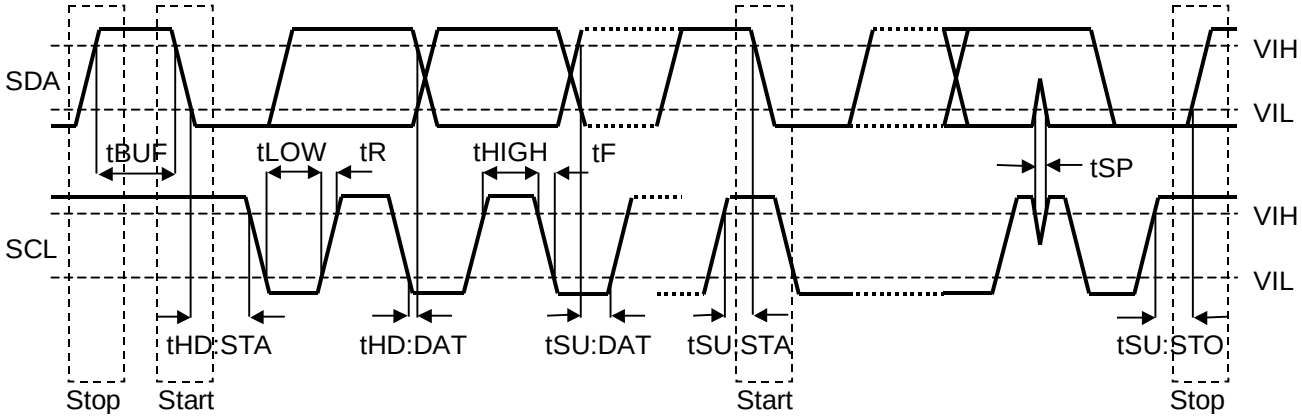


Figure 52. I²C Bus Control Mode Timing

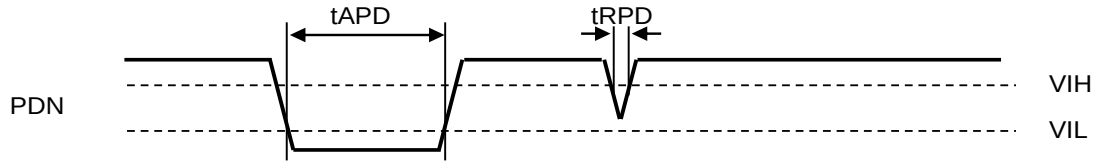


Figure 53. Power Down & Reset Timing

9. Functional Descriptions

9.1. Data Conversion Mode

The AK4191 is able to convert either PCM or DSD data to a multi-bit stream signal. In PCM mode, clocks and PCM data can be input from the BICK, LRCK, SDATA and SDATA2 pins. In DSD mode, clocks and DSD data can be input from the DCLK, DSDL and DSDR pins when DSDPATH bit = ”1”, and the DCLK2, DSDL2 and DSDR2 pins when DSDPATH bit = ”0”.
.

The AK4191 supports external Digital Filter I/F (EXDF) in PCM data input mode. In EXDF mode, clocks and PCM data can be input from the BCK, WCK, DINL/L2 and DINR/R2 pins. Table 1 shows available functions in PCM/DSD/EXDF mode.

Table 1. Function List of PCM/EXDF/DSD Mode
(Y: Available, N/A: Not available)

Function	Default State	Addr	Bit	PCM	EXDF	DSD
MCLK Output	Disable	08H	MCKOE	Y	Y	Y
MCLK Output Divider	OFF	08H	MCKDV	Y	Y	Y
RSTN	Reset	00H	RSTN	Y	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	Y	N/A
Data Synchronization Function	Disable	0BH	DSYNCE	Y	Y	Y (Note 22)
Automatic Mode Switching (PCM/DSD, EXDF/DSD)	Disable	15H	ADPE	Y	Y	Y
Automatic System clock setting @DSD mode	Disable	02H	ADCKS	N/A	N/A	Y
System clock setting for Master mode	64fs	00H	DFS [2:0]	Y	Y	N/A
De-emphasis Response	OFF	01H	DEM [1:0]	Y	N/A	N/A
TDM Interface Format	Normal Mode	0AH	TDM [1:0]	Y	N/A	N/A
Digital Filter select @PCM mode	Short Delay Sharp Roll-off filter	01H	SSLOW, SD, SLOW	Y (Note 21)	Y (Note 21)	N/A
Audio Data Interface Format @ PCM mode	32-bit MSB	00H	DIF [2:0]	Y	N/A	N/A
Audio Data Interface Format @ EXDF mode	32-bit LSB	00H	DIF [2:0]	N/A	Y	N/A
DUAL Input mode @ PCM mode, EXDF mode	Disable	00H	DUAL	Y	Y	N/A
Digital Filter select @DSD mode	39 kHz filter	09H	DSDF	N/A	N/A	Y
Path select @ DSD mode	Normal Path	06H	DSDD	N/A	N/A	Y
DSD Mute Function @ Full-scale Detected	Disable	06H	DDM	N/A	N/A	Y

Note 21. When Sampling Speed Mode is 32×, only Sharp Roll-off Filter is supported.
Note 22. This function is not available when DSDD bit = “1”.

Function	Default State	Addr	Bit	PCM	EXDF	DSD
Gain Adjustment	56% (Note)	07H	GC [3:0]	Y	Y	Y (Note 22)
Attenuation Level	0 dB	03H 04H	ATTL [7:0] ATTR [7:0]	Y	Y	Y (Note 22)
Soft Mute	Mute off	01H	SMUTE	Y	Y	Y (Note 22)
Data Zero Detection or DSD Full scale Detection Flag Output	Disable	02H	DZFE DDMOE	Y	Y	Y
Inverting Enable of DZF	“H” active	02H	DZFB	Y	Y	Y
Mono/Stereo mode select	Stereo	05H	MONO	Y	Y	Y
Data Invert mode select	OFF	05H	INVL/R	Y	Y	Y
The data selection of L channel and R channel	L/R channel	05H	SELLR	Y	Y	Y
MBD Zero Output Function	Disable	0CH	MBDZ	Y	Y	Y
MUTEN condition setting	Full function	00H	MUTES [1:0]	Y	Y	Y
DSM Data Mix Function	Disable	0DH	PMDSMI	Y	Y	Y (Note 22)
DSM Data Mix Polarity	Add	0DH	SUBL/R	Y	Y	Y (Note 22)
Bit Number Select for DSM Data Mix Input	7bits	0DH	IBIT	Y	Y	Y (Note 22)
Attenuation Level for DSM Data Mix	MUTE (∞)	0EH 0FH	ATTMXL [7:0] ATTMXR [7:0]	Y	Y	Y (Note 22)
Delta-Sigma Option	Type1	0DH	DSMSEL [1:0]	Y	Y	Y (Note 22)

Note. This reference is input signal, input signal is 100%.

9.1.1. Data Conversion Mode Setting and Pin Assignment

Switching to DSD mode, manual and automatic settings are selectable. The AK4191 is in Manual Setting Mode when ADPE bit = “0” and it is in Automatic Setting Mode when ADPE bit = “1”.

In Manual setting mode (ADPE bit = “0”), PCM/DSD/EXDF mode is executed by setting DP bit and EXDF bit. The AK4191 enters PCM mode by setting DP bit = “0” and EXDF bit = ”0”, the AK4191 enters DSD mode by setting DP bit = “1”, The AK4191 enters EXDF mode by setting DP bit = “0” and EXDF bit = “1”. In DSD mode, EXDF bit setting will not be reflected on the circuit operation.

In Auto Setting Mode (ADPE bit = “1”), PCM/DSD automatic switching mode is enabled when EXDF bit = “0”, EXDF/DSD automatic switching mode is enabled when EXDF bit = “1”. DP bit setting is ignored. The AK4191 monitors input signals to select PCM/DSD or EXDF/DSD mode. Refer to “9.10. Automatic Data Conversion Mode Switching” for details of PCM/DSD mode automatic switching

・PCM Mode
Clock and data are input to the #2, #3, #4 and #5 pins in PCM mode (Table 3).

・DSD Mode
Clock and data input pin can be changed by DSDPATH bit. Clock and data are input to the #8, #9 and #10 pins if DSDPATH bit = “0”, and are input to the #2, #3 and #4 pins if DSDPATH bit = “1” (Table 3).

・EXDF Mode
Clock and data are input to the #2, #3, #4, #5, #6 and #7 pins in EXDF mode (Table 3).

Table 2. PCM/DSD/EXDF Mode Control (×: Do Not Care)

ADPE bit	DP bit	EXDF bit	Data Conv. Mode
0	0	0	PCM
		1	EXDF
	1	×	DSD
1	×	0	PCM or DSD
		1	EXDF or DSD

Table 3. PCM/DSD/EXDF Pin Assign (×: Do Not Care)

Data Conv. Mode	DSD PATH bit	Pin Assignment								
		#2	#3	#4	#5	#6	#7	#8	#9	#10
PCM	×	BICK	SDATA	LRCK	SDATA2	Not Used	Not Used	Not Used	Not Used	Not Used
EXDF	×	BCK	DINL	DINR	DINL2	DINR2	WCK	Not Used	Not Used	Not Used
DSD	0	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	DSDL2	DSDR2	DCLK2
	1	DCLK	DSDL	DSDR	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

9.1.2. Data Conversion Mode Switching Timing (Manual Setting)

In manual setting mode (ADPE bit = “0”), the AK4191 must be in reset state by setting RSTN bit = “0” when switching the data input mode (PCM/DSD/EXDF) by DP bit and EXDF bit or when changing DSD signal input path by DSDPATH bit. RSTN bit should not be changed for 4/fs after switching these modes. It takes 2/fs to 3/fs for mode transition.

Figure 54, Figure 55 and Figure 56 show switching timing of PCM, DSD and EXDF modes in manual mode (ADPE bit = “0”). To prevent noise caused by excessive input, DSD signal should be input 4/fs after setting RSTN bit = “0” until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM/EXDF mode. DSD signal should be stopped 4/fs after setting RSTN bit = “0” until the device is completely reset internally when the conversion mode is changed to PCM/EXDF from DSD mode.

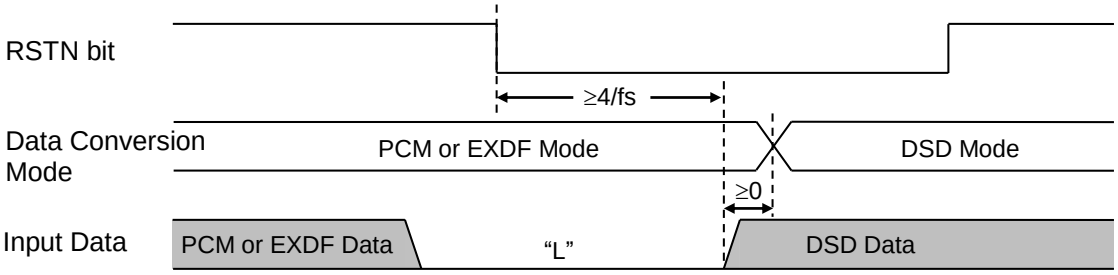


Figure 54. D/A Mode Switching Timing (from PCM/EXDF Mode to DSD Mode)

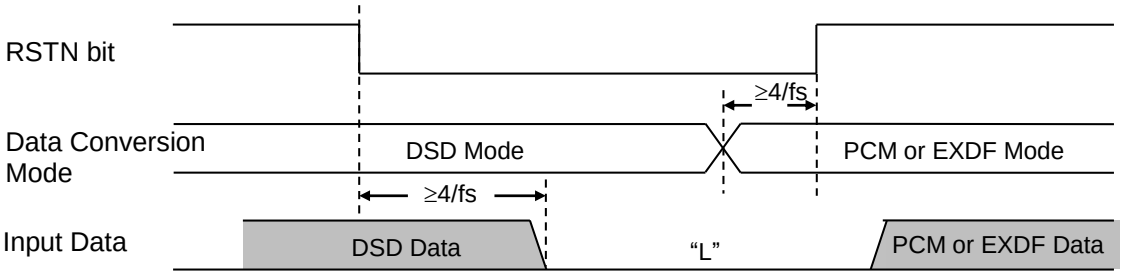


Figure 55. D/A Mode Switching Timing (from DSD Mode to PCM/EXDF Mode)

Figure 56 shows switching timing of PCM and EXDF modes. Set EXDF bit 4/fs after setting RSTN bit = “0” until the device is completely reset internally when changing the conversion mode.

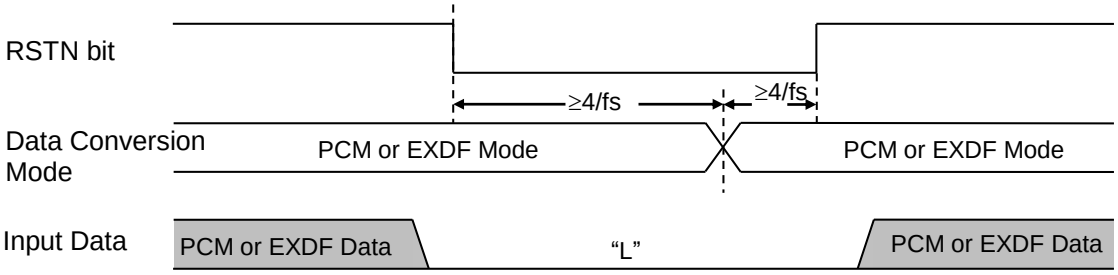


Figure 56. D/A Mode Switching Timing (from PCM Mode to EXDF Mode)

9.1.3. Playback Mode

9.1.3.1. Asynchronous and Synchronous Modes

The AK4191 has Data Synchronization circuit to play back asynchronous audio signal inputs. Asynchronous Mode is enabled by setting DSYNCE bit = ”1”. In this mode, the AK4191 synchronize the audio signal input via SDATA, SDATA2, DINL, DINR, DINL2, DINR2, DSDL, DSDR, DSDL2 and DSDR2 pins to a clock input via MCLK pin. The sampling frequency of audio signal input only for 44.1 kHz and 48 kHz base rates are supported. So, the sampling frequency setting FS32K bit should be “0”. This function is disabled and the Data Synchronization circuit is powered down when setting DSYNCE bit = ”0” (Table 4).

Table 4. Playback Mode Selection

DSYNCE	Mode	
0	Synchronous Mode	(default)
1	Asynchronous Mode	

The base sampling frequency range is 43.7kHz to 44.5kHz when base rate is 44.1kHz, and 47.6kHz to 48.4kHz when base rate is 48kHz in this mode. Pop noise may occur if the base sampling frequency exceeds this range. The digital filter setting SLOW bit and SSLOW bit are recommended to be “0” when PCM or EXDF mode are selected, and the DSD playback path setting DSDD bit should be “0”.

The Data Synchronization circuit has a FIFO. Therefore, the data output delay when DSYNCE bit = ”1” becomes 0.5/fso to 3.5/fso larger or small than when DSYNCE bit = “0” (Table 5). Here, fso means Base MCLK Frequency/256.

Table 5. Data Output Delay

DSYNCE	Data Output Delay	
0	“GD” shown in 8.2. Digital Filter Characteristics	(default)
1	“GD” + 0.5/fso to “GD” + 3.5/fso	

9.1.3.2. DSD Volume Bypass Mode

The AK4191 has a Volume bypass function for playing back a DSD signal. Two modes are selectable by DSDD bit (Table 6). When setting DSDD bit = “1”, the output volume control function is not available.

Table 6. DSD Playback Path Selection

DSDD	Mode	
0	Normal Path	(default)
1	Volume Bypass	

9.2. System Clock

9.2.1. Master Clock (MCLK)

9.2.1.1. MCLK input

The external Master Clock (MCLK) must be input via MCLKI pin to operate the AK4191. MCLK must be continuous, not burst mode. The frequency of MCLK should be changed during PMPLL bit = “0”. There are four system clock setting modes controlled by MCKS [1:0] bits (Table 7). FS32K bit must be set “1” when base sampling frequency is 32kHz. FS32K bit and MCKS[1:0] bits should be set before setting PMPLL bit = “1”.

Table 7. System Clock Setting Mode

MCKS [1:0] bits	MCLK frequency [MHz]			
	FS32K bit = ”0”		FS32K bit = ”1”	
	48 kHz base	44.1 kHz base	32 kHz base	
00	12.288	11.2896	8.192	(default)
01	24.576	22.5792	16.384	
10	3.072	2.8224	2.048	
11	6.144	5.6448	4.096	

9.2.1.2. Internal Master Clock

The AK4191 integrates PLL and generates internal master clock from the input clock of the MCLKI pin. PLL multiple number is determined by FS32K bit and MCKS [1:0] bits that are for MCLK frequency setting (Table 7). When PLL reset is released (PMPLL bit = “1”), the internal PLL starts operation and generates a 98.304 MHz, 90.3168 MHz or 65.536 MHz internal master clock (PLLCK) by multiplying MCLK.

Table 8. Internal Master Clock

Internal Master Clock (PLLCK) Frequency	FS32K bit = ”0”		FS32K bit = ”1”
	48 kHz base	44.1 kHz base	32 kHz base
	98.304 MHz	90.3168 MHz	65.536 MHz

When the frequency of the internal Master Clock (PLLCK) is unstable, the AK4191 will stop operation and output “L” to MBD7-1 pins. In this state, it is possible to output status flag to MUTEN pin or force data of MBD7-1 pins output “L” state automatically. Refer to 9.12. Mute signal output.

9.2.2. Delta Sigma Modulator Data Output Frequency Setting (BCKO, OSR bit)

The AK4191 outputs BCKO to transfer MBD7-1 data. This clock is generated by using internal Master Clock (PLLCK). The output frequencies are shown in Table 9.
When the frequency of the internal Master Clock (PLLCK) is unstable, the AK4191 outputs “L” to BCKO pin.

Table 9. BCKO Frequency setting

OSR bits	BCKO frequency [MHz]		
	48 kHz base	44.1 kHz base	
0	12.288	11.2896	(default)
1	6.144	5.6448	

9.2.3. PCM Mode

Two PCM audio clock modes, such as slave mode and master mode, are available. The AK4191 is in Slave mode when setting MSN bit “0” and it is in Master Mode when setting MSN bit = “1”.

9.2.3.1. Slave Mode (MSN bit = ”0”)

In slave mode, the external BICK and LRCK are required. The AK4191 will detect the MCLK and LRCK frequency ratio to set the sampling speed mode automatically. Therefore, sampling speed setting is not necessary. The frequencies of LRCK corresponding to each sampling speed mode should be input externally (Table 10).

Table 10. LRCK frequency and Sampling Speed Mode

48 kHz base			44.1 kHz base			Sampling Speed Mode
LRCK frequency	Base MCLK Frequency		LRCK frequency	Base MCLK Frequency		
	DSYNCE = ”0”	DSYNCE = ”1”		DSYNCE = ”0”	DSYNCE = ”1”	
48.0 kHz	12.288 MHz	11.2896 MHz or 12.288MHz	44.1 kHz	11.2896 MHz	11.2896 MHz or 12.288MHz	1×
96.0 kHz			88.2 kHz			2×
192.0 kHz			176.4 kHz			4×
384.0 kHz			352.8 kHz			8×
768.0 kHz			705.6 kHz			16×
1536.0 kHz			1411.2 kHz			32×

In Synchronous Mode (DSYNCE bit = “0”), MCLK, BICK and LRCK should be synchronized but the phase of MCLKs not critical. In Asynchronous Mode (DSYNCE bit =”1”), BICK and LRCK should be synchronized but MCLK should not be synchronized to BICK and LRCK.
Auto detection result of the sampling speed can be read out by ADFS [2:0] bits (Table 11).

Table 11. Relationship between ADFS [2:0] bits and Sampling Speed Mode

ADFS [2:0] bits Read Result	Sampling Speed Mode
000	1×
001	2×
010	4×
011	4×
100	8×
101	16×
110	32×
111	32×

9.2.3.2. Master Mode (MSN bit = “1”)

In master mode, the AK4191 outputs BICK and LRCK. These clocks are generated by internal PLL and synchronized to MCLK in this mode, the AK4191 supports only Synchronous Mode (DSYNCE = ”0”) and audio interface format mode is limited only PCM Normal Mode (TDM [1:0] bits = “00”).
Sampling speed setting of LRCK and speed setting of BICK should be selected by DFS [2:0] bits and BCKS [1:0] bits as shown in Table 12 and Table 13.

Table 12. PCM Audio Clock Outputs Example (44.1 kHz base) (N/A: Not Available)

DFS [2:0] bits	LRCK frequency [kHz]	BICK frequency [MHz]		
		BCKS [1:0] bits		
		00	01	10/11
	Fs	128fs	64fs	32fs
000	44.1 kHz	5.6448	2.8224	1.4112
001	88.2 kHz	11.2896	5.6448	2.8224
010/011	176.4 kHz	22.5792	11.2896	5.6448
100	352.8 kHz	45.1584	22.5792	11.2896
101	705.6 kHz	N/A	45.1584	22.5792
110/111	1411.2 kHz	N/A	N/A	45.1584

Table 13. PCM Audio Clock Outputs Example (48 kHz base) (N/A: Not Available)

DFS [2:0] bits	LRCK frequency [kHz]	BICK frequency [MHz]		
		BCKS [1:0] bits		
		00	01	10/11
	Fs	128fs	64fs	32fs
000	48.0 kHz	6.144	3.072	1536
001	96.0 kHz	12.288	6.144	3.072
010/011	192.0 kHz	24.576	12.288	6.144
100	384.0 kHz	49.152	24.576	12.288
101	768.0 kHz	N/A	49.152	24.576
110/111	1536.0 kHz	N/A	N/A	49.152

9.2.4. DSD Mode

The external DCLK is required in DSD mode. In Synchronous Mode (DSYNCE bit = “0”), DCLK should be synchronized with MCLK but the phase is not critical. The AK4191 supports DSD data stream rates of DSD64, DSD128, DSD256, DSD512 and DSD1024 modes. Two modes for setting DSD data stream rates are selectable by ADCKS bit.

9.2.4.1. Manual Setting Mode (ADCKS bit = ”0”)

The AK4191 supports DSD data stream rates of 2.8224 MHz (64fs), 5.6448 MHz (128fs), 11.2896 MHz (256fs), and 22.5792 MHz (512fs) for 44.1 kHz base rates. In Synchronous Mode (DSYNCE bit = “0”), any base rate in the range 30 kHz to 48 kHz is supported. The data sampling speed is selected by DSDSEL [2:0] bits (Table 14). In Synchronous Mode (DSYNCE bit = “0”), DCLK and MCLK should be synchronized but the phase is not critical. In Asynchronous Mode (DSYNCE bit =”1”), DCLK should not be synchronized to MCLK.

Table 14. DSD Audio Clock Frequency Example (ADCKS bit =”0”)

DSDSEL [2:0] bits	DSD mode	48 kHz base			44.1 kHz base			
		DCLK frequency [MHz]	Base MCLK Frequency [MHz]		DCLK frequency [MHz]	Base MCLK Frequency [MHz]		
			DSYNCE = ”0”	DSYNCE = ”1”		DSYNCE = ”0”	DSYNCE = ”1”	
000	DSD64	3.072	12.288	11.2896 or 12.288	2.8224	11.2896	11.2896 or 12.288	(default)
001	DSD128	6.144			5.6448			
010	DSD256	12.288			11.2896			
011	DSD512	24.576			22.5792			
100/101/ 110/111	DSD1024	49.152			45.1584			

9.2.4.2. Auto Setting Mode (ADCKS bit = ”1”)

The AK4191 will detect the MCLK and DCLK frequency ratio to set the DSD data stream rate mode automatically. Therefore, DSD data stream rate setting is not necessary. Auto detection result of the data stream rate can be read out by ADSDS [2:0] bits (Table 15). In Synchronous Mode (DSYNCE bit = “0”), DCLK and MCLK should be synchronized but the phase is not critical. In Asynchronous Mode (DSYNCE bit =”1”), DCLK should not be synchronized to MCLK.

Table 15. Relationship between ADSDS [2:0] bits and DSD Clock Rate

ADSDS [2:0] Read Results	DSD mode	48 kHz base			44.1 kHz base			
		DCLK frequency [MHz]	Base MCLK Frequency [MHz]		DCLK frequency [MHz]	Base MCLK Frequency [MHz]		
			DSYNCE = ”0”	DSYNCE = ”1”		DSYNCE = ”0”	DSYNCE = ”1”	
000	DSD64	3.072	12.288	11.2896 or 12.288	2.8224	11.2896	11.2896 or 12.288	(default)
001	DSD128	6.144			5.6448			
010	DSD256	12.288			11.2896			
011	DSD512	24.576			22.5792			
100/101/ 110/111	DSD1024	49.152			45.1584			

9.2.5. External Digital Filter Mode (EXDF Mode)

Two EXDF audio clock modes, such as slave mode and master mode, are available. The AK4191 is in Slave mode when setting MSN bit “0” and it is in Master Mode when setting MSN bit = “1”.

9.2.5.1. Slave Mode (MSN bit = ”0”)

In slave mode, the external clocks that are required in EXDF mode are BCK and WCK. The BCK must be continuous, not burst mode.

The AK4191 will detect the MCLK and WCK frequency ratio to set the sampling speed mode automatically. Therefore, sampling speed setting is not necessary. The frequencies of WCK corresponding to each sampling speed mode should be input externally (Table 16). In Synchronous Mode (DSYNCE bit = “0”), MCLK, BCK and WCK should be synchronized but the phase of MCLKs not critical. In Asynchronous Mode (DSYNCE bit = “1”), BCK and WCK should be synchronized.

Table 16. WCK frequency and Sampling Speed Mode

48 kHz base			44.1 kHz base			Sampling Speed Mode
WCK frequency	Base MCLK Frequency		WCK frequency	Base MCLK Frequency		
	DSYNCE = ”0”	DSYNCE = ”1”		DSYNCE = ”0”	DSYNCE = ”1”	
384.0 kHz	12.288 MHz	11.2896 MHz or 12.288MHz	352.8 kHz	11.2896 MHz	11.2896 MHz or 12.288MHz	8×
768.0 kHz			705.6 kHz			16×
1536.0 kHz			1411.2 kHz			32×

Auto detection result of the sampling speed can be read out by ADFS [2:0] bits (Table 11).

9.2.5.2. Master Mode (MSN bit = “1”)

In master mode, the AK4191 outputs BCK and WCK. These clocks are generated by internal PLL and synchronized to MCLK. In this mode, the AK4191 supports only Synchronous Mode (DSYNCE = ”0”) and audio interface format mode is limited only PCM Normal Mode (TDM [1:0] bits = “00”).
Sampling speed setting of WCK and speed setting of BCK should be selected by DFS [2:0] bits and BCKS [1:0] bits as shown in Table 17 and Table 18.

Table 17. EXDF Audio Clock Outputs Example (44.1 kHz base) (N/A：Not Available)

DFS [2:0] bits	WCK frequency [kHz]	BCK frequency [MHz]		
		BCKS [1:0] bits		
		00	01	10/11
	fs	128fs	64fs	32fs
100	352.8 kHz	45.1584	22.5792	11.2896
101	705.6 kHz	N/A	45.1584	22.5792
110/111	1411.2 kHz	N/A	N/A	45.1584

Table 18. EXDF Audio Clock Outputs Example (48 kHz base) (N/A：Not Available)

DFS [2:0] bits	WCK frequency [kHz]	BCK frequency [MHz]		
		BCKS [1:0] bits		
		00	01	10/11
	fs	128fs	64fs	32fs
100	384.0 kHz	49.152	24.576	12.288
101	768.0 kHz	N/A	49.152	24.576
110/111	1536.0 kHz	N/A	N/A	49.152

9.2.6. Delta Sigma Modulator Data Input Frequency Setting (BCKI)

The external BCKI is required when PMDSMI bit =”1”. MCLK should be synchronized with BCKI but the phase is not critical. The AK4191 supports DSMI data stream rates of 128fs and 256fs modes. Two modes for setting DSMI1-7 data stream rates are selectable by DSMIFS bit.
DSMIFS bit should be “1” when setting OSR bit is “1”.

Table 19. BCKI Frequency setting

DSMIFS bits	BCKI frequency [MHz]		
	48 kHz base	44.1 kHz base	
0	12.288	11.2896	(default)
1	6.144	5.6448	

9.3. Audio Input Interface Format

9.3.1. PCM Mode

Four data modes, such as Normal Mode, TDM128, TDM256, and TDM512 Modes, are available. Mode settings are available by the registers (TDM [1:0] bits and DIF [2:0] bits). However, it should not be changed during operation. The AK4191 must be reset by setting RSTN bit when the format setting is changed during operation.

9.3.1.1. Input Data Format

Normal Mode (TDM [1:0] bits = "00")

【Single Input Mode (DUAL bit ="0")】
Stereo Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF [2:0] bits as shown in Table 20. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 16-bit and 20-bit, Mode 6 can be used for 16-bit, 20-bit and 24-bit MSB justified formats by zeroing the unused LSBs. DIF [2:0] bits should be "000" when Sampling Speed mode is 32×.

【Dual Input Mode (DUAL bit ="1")】
Stereo Data is shifted in via the SDATA, SDATA2 pins using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF [2:0] bits as shown in Table 20. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK. Mode 2 can be used for 32-bit and 40-bit, Mode 6 can be used for 32-bit, 40-bit and 48-bit MSB justified formats by zeroing the unused LSBs. DIF [2:0] bits should be "000" when Sampling Speed mode is 32×.

TDM128 Mode (TDM [1:0] bits = "01")

Up to 4-ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Input data to the SDATA2 pin will be ignored. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF [2:0] bits as shown in Table 20. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM256 Mode (TDM [1:0] bits = "10")

Up to 8-ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Input data to the SDATA2 pin will be ignored. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF [2:0] bits as shown in Table 20. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

TDM512 Mode (TDM [1:0] bits = "11")

Up to 16-ch Data is shifted in via the SDATA pin using BICK and LRCK inputs. Input data to the SDATA2 pin is ignored. BICK is fixed to 512fs. Six data formats are supported and selected by the DIF [2:0] bits as shown in Table 20. In all formats the serial data is MSB first, 2's compliment format and is read on the rising edge of BICK.

Table 20. Audio Interface Format

Mode		TDM [1:0] bits	DIF [2:0] bits	SDATA, SDATA2 Format	LRCK	BICK	Figure	
Normal Single (Note 23)	0	00	000	16-bit LSB justified	H/L	≥32fs	Figure 57	
	1		001	20-bit LSB justified	H/L	≥40fs	Figure 58	
	2		010	24-bit MSB justified	H/L	≥48fs	Figure 59	
	3		011	16-bit I²S compatible	L/H	32fs	Figure 60	
				24-bit I²S compatible	L/H	≥48fs		
	4		100	24-bit LSB justified	H/L	≥48fs	Figure 58	
	5		101	32-bit LSB justified	H/L	≥64fs	Figure 61	
	6		110	32-bit MSB justified	H/L	≥64fs	Figure 62	(default)
	7		111	32-bit I²S compatible	L/H	≥64fs	Figure 63	
Normal Dual (Note 23)	0	00	000	32-bit LSB justified	H/L	≥32fs	Figure 57	
	1		001	40-bit LSB justified	H/L	≥40fs	Figure 58	
	2		010	48-bit MSB justified	H/L	≥48fs	Figure 59	
	3		011	32-bit I²S compatible	L/H	32fs	Figure 60	
				48-bit I²S compatible	L/H	≥48fs		
	4		100	48-bit LSB justified	H/L	≥48fs	Figure 58	
	5		101	64-bit LSB justified	H/L	≥64fs	Figure 61	
	6		110	64-bit MSB justified	H/L	≥64fs	Figure 62	
	7		111	64-bit I²S compatible	L/H	≥64fs	Figure 63	
TDM128		01	000	N/A	-	-	-	
			001	N/A	-	-	-	
	8		010	24-bit MSB justified	H/L	128fs	Figure 64	
	9		011	24-bit I²S compatible	L/H	128fs	Figure 65	
	10		100	24-bit LSB justified	H/L	128fs	Figure 66	
	11		101	32-bit LSB justified	H/L	128fs	Figure 64	
	12		110	32-bit MSB justified	H/L	128fs	Figure 64	
	13		111	32-bit I²S compatible	L/H	128fs	Figure 65	
TDM256		10	000	N/A	-	-	-	
			001	N/A	-	-	-	
	14		010	24-bit MSB justified	H/L	256fs	Figure 67	
	15		011	24-bit I²S compatible	L/H	256fs	Figure 68	
	16		100	24-bit LSB justified	H/L	256fs	Figure 69	
	17		101	32-bit LSB justified	H/L	256fs	Figure 67	
	18		110	32-bit MSB justified	H/L	256fs	Figure 67	
	19		111	32-bit I²S compatible	L/H	256fs	Figure 68	
TDM512		11	000	N/A	-	-	-	
			001	N/A	-	-	-	
	20		010	24-bit MSB justified	H/L	512fs	Figure 70	
	21		011	24-bit I²S compatible	L/H	512fs	Figure 71	
	22		100	24-bit LSB justified	H/L	512fs	Figure 72	
	23		101	32-bit LSB justified	H/L	512fs	Figure 70	
	24		110	32-bit MSB justified	H/L	512fs	Figure 70	
	25		111	32-bit I²S compatible	L/H	512fs	Figure 71	

Note 23. The cycle numbers of BICK for each channel must be the same as the bit length setting or more. L channel data can be input when LRCK = “H” and R channel data can be input when LRCK = “L” if the LRCK indication is “H/L”. L channel data can be input when LRCK = “L” and R channel data can be input when LRCK = “H” if the LRCK indication is “L/H”.

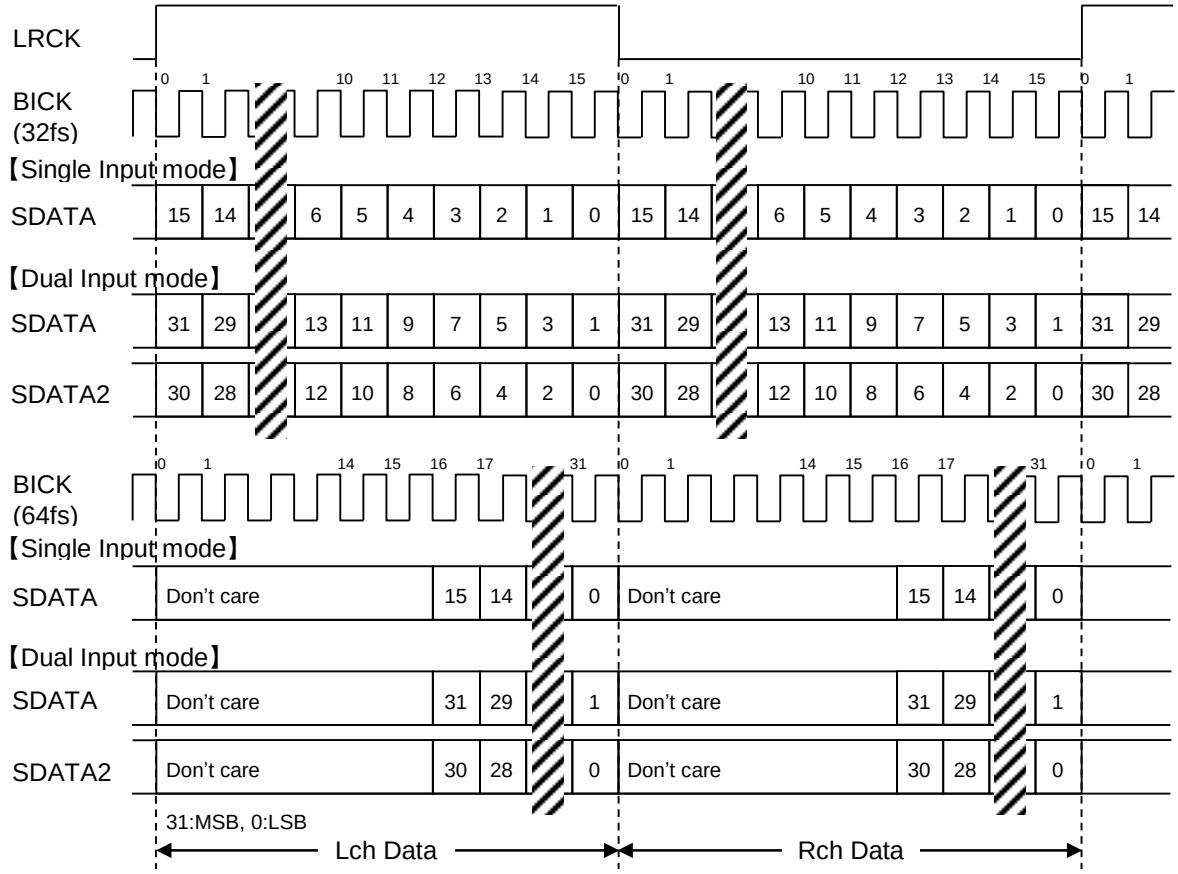


Figure 57. Mode 0 Timing

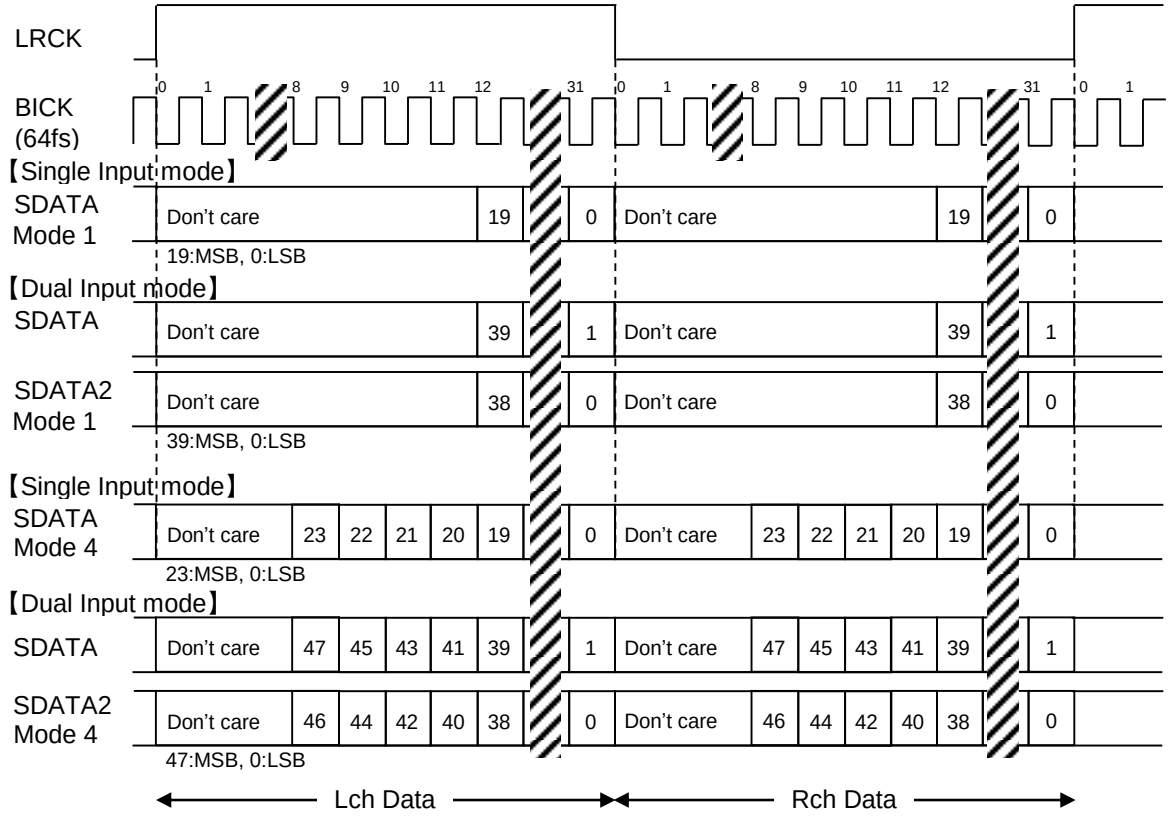


Figure 58. Mode 1, 4 Timing

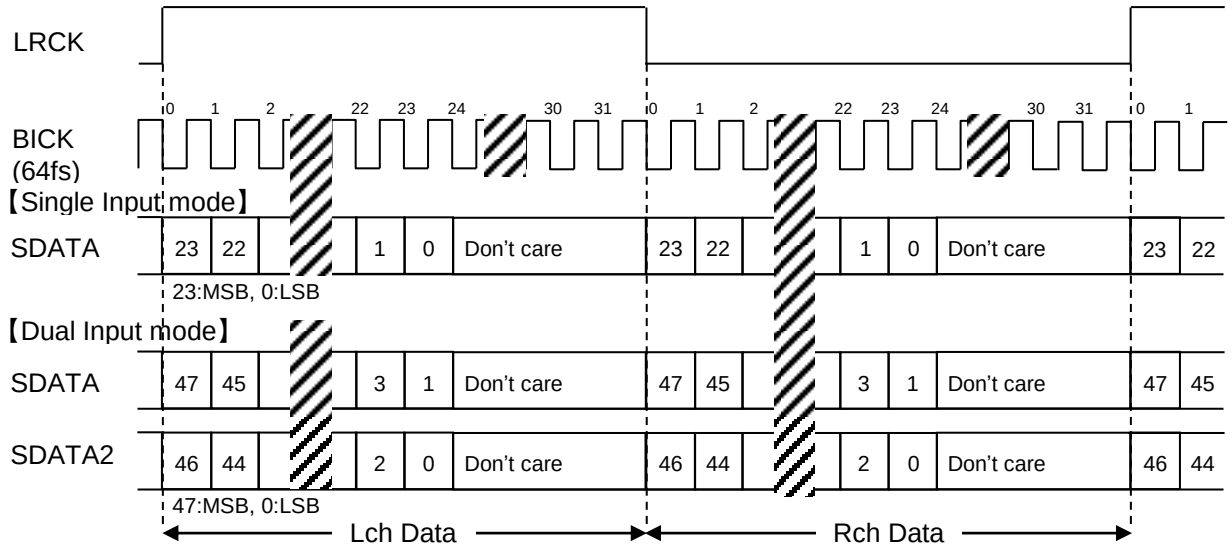


Figure 59. Mode 2 Timing

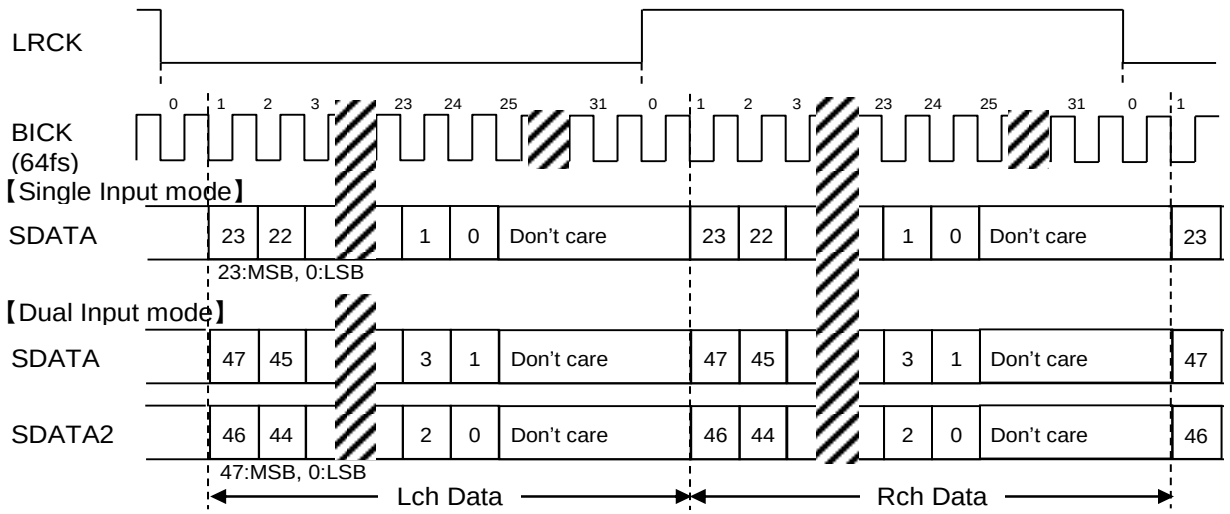


Figure 60. Mode 3 Timing

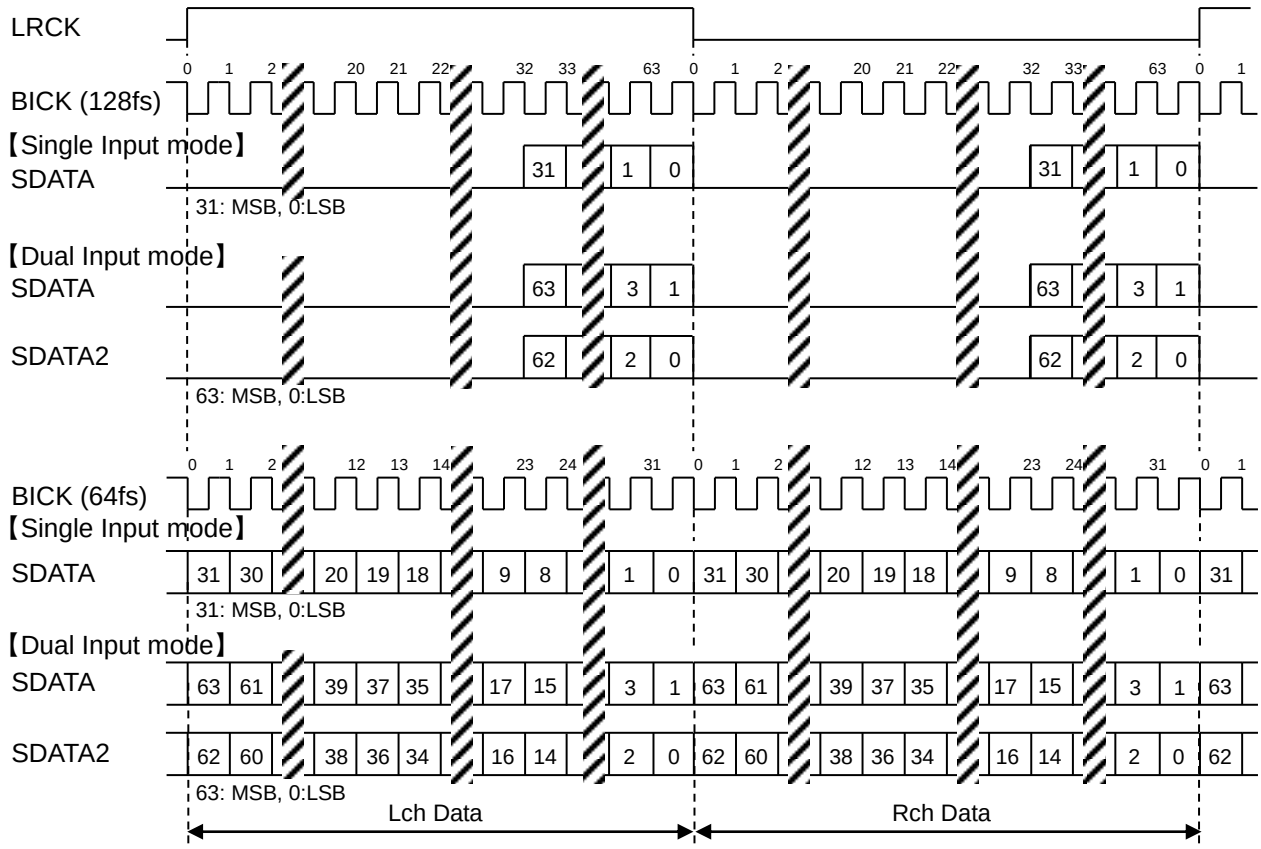


Figure 61. Mode 5 Timing

Figure 62. Mode 6 Timing

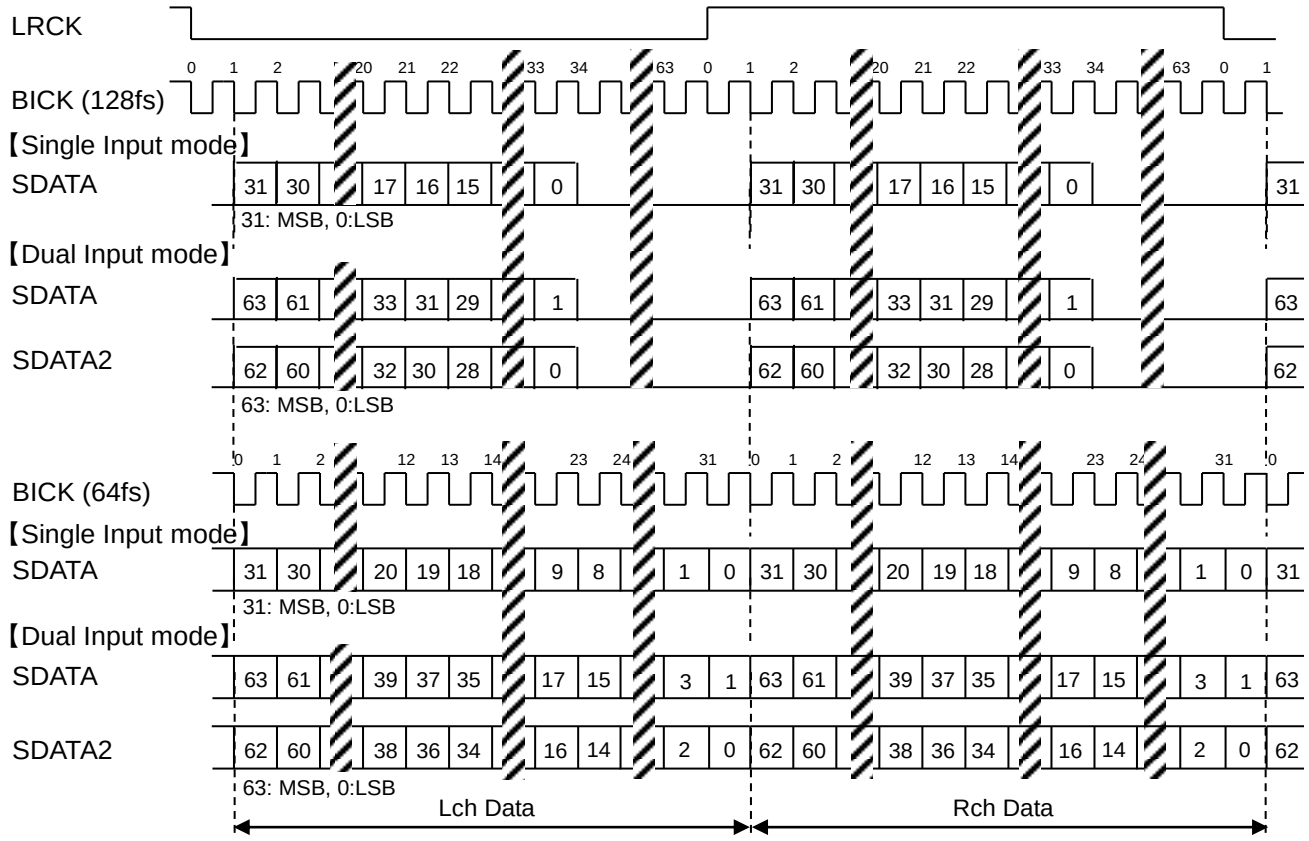


Figure 63. Mode 7 Timing

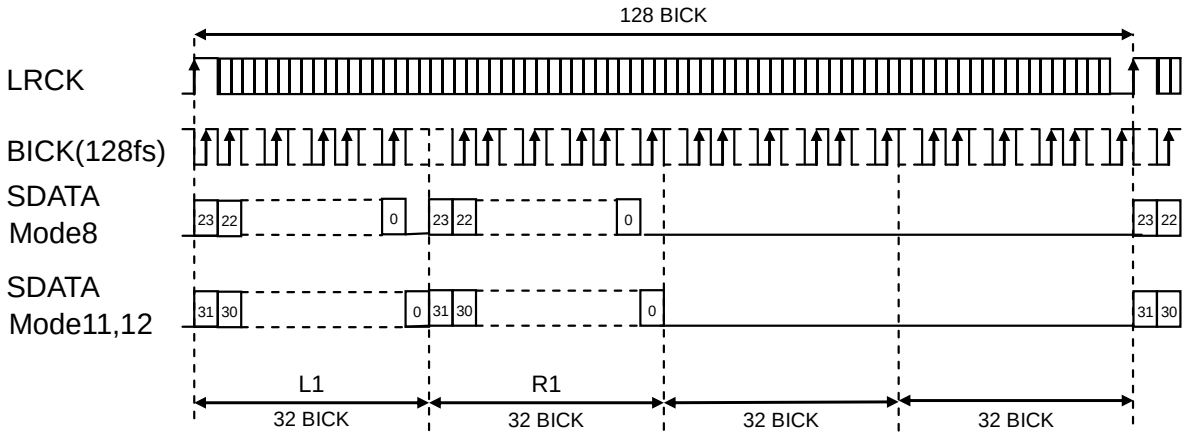


Figure 64. Mode 8/11/12 Timing

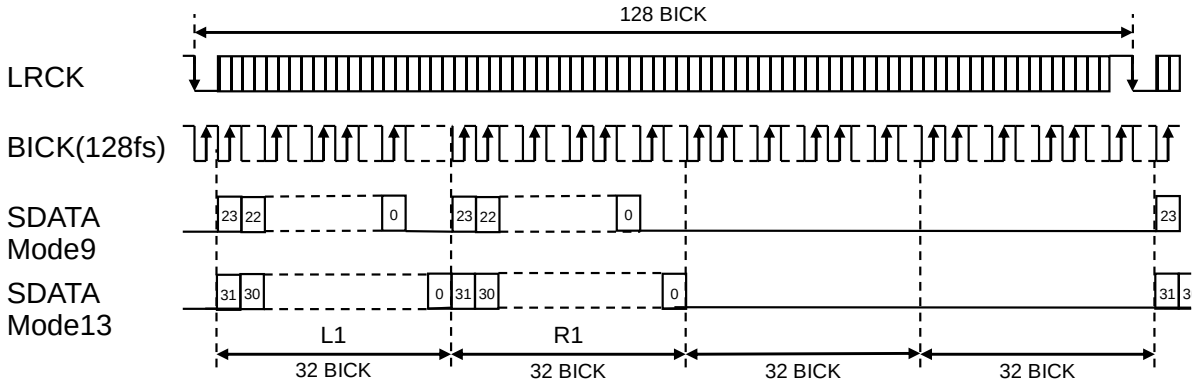


Figure 65. Mode 9/13 Timing

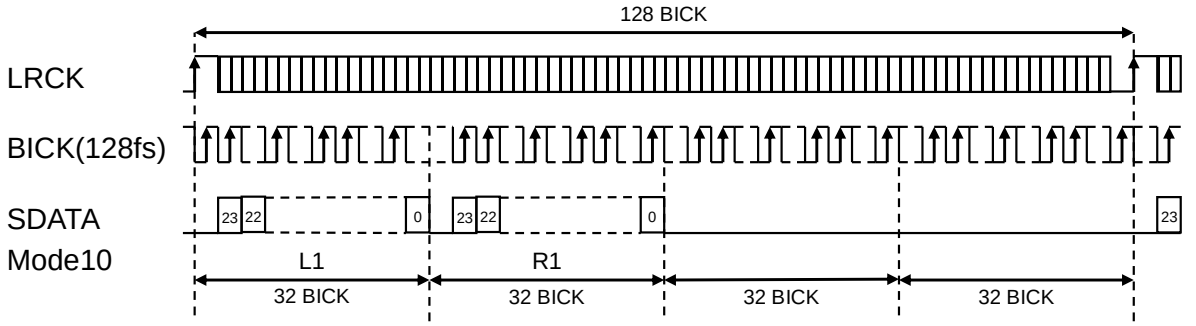


Figure 66. Mode 10 Timing

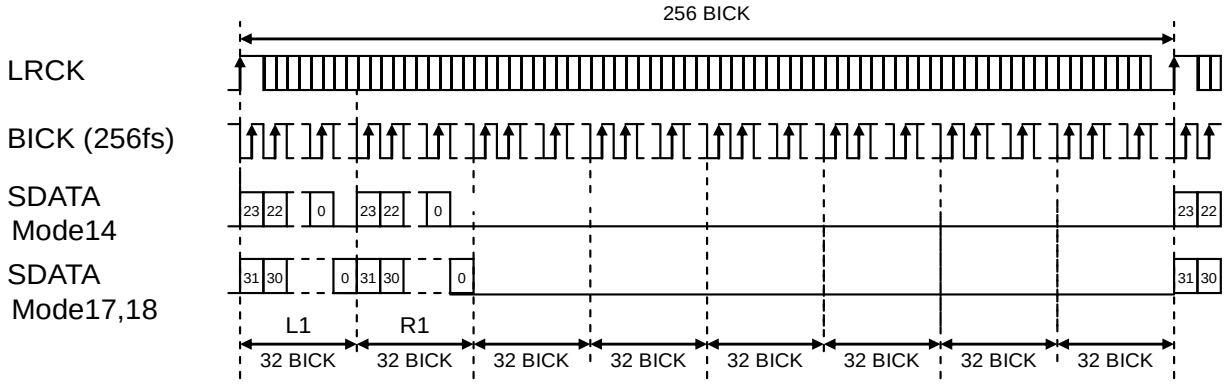


Figure 67. Mode 14/17/18 Timing

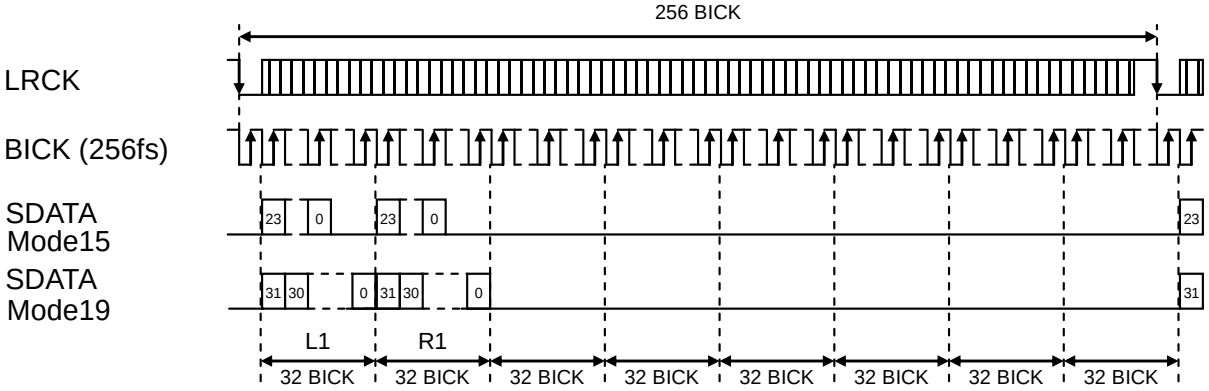


Figure 68. Mode 15/19 Timing

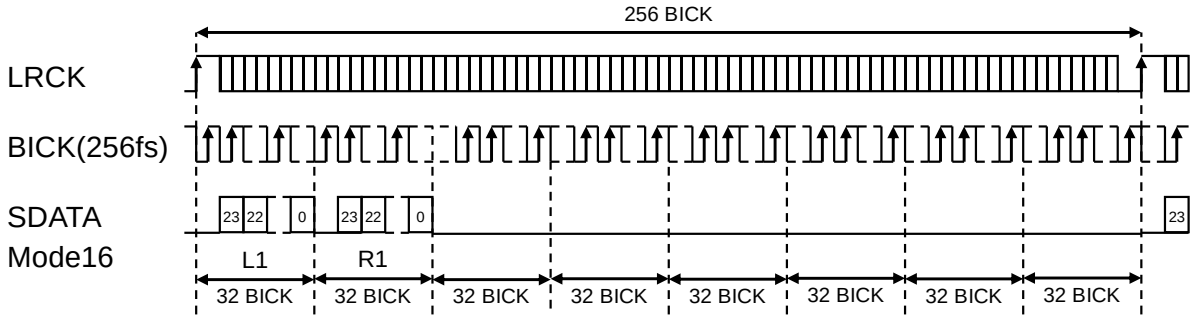


Figure 69. Mode 16 Timing

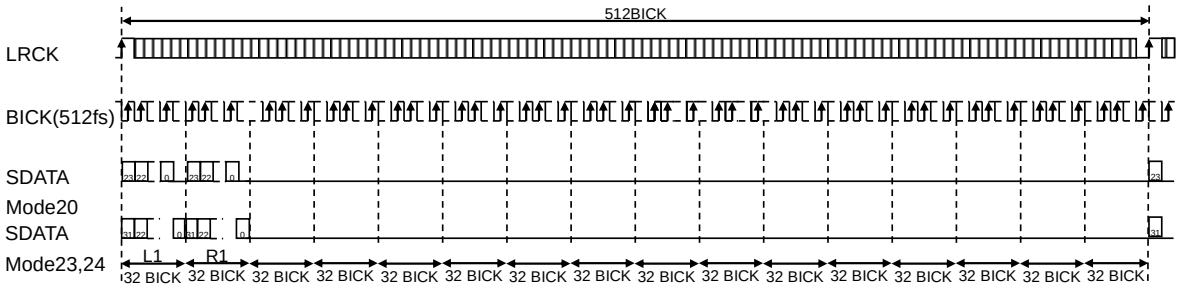


Figure 70. Mode 20/23/24 Timing

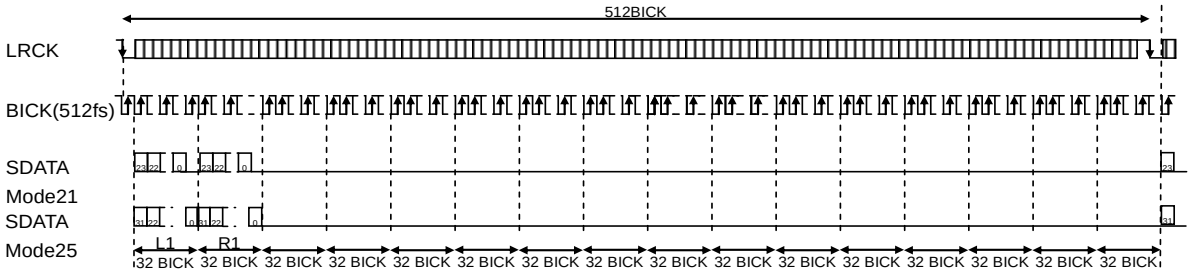


Figure 71. Mode 21/25 Timing

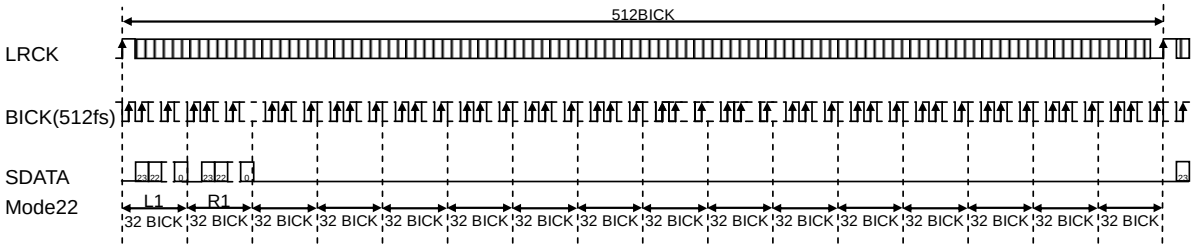


Figure 72. Mode 22 Timing

9.3.1.2. Data Slot Selection Function

Data slot of 1cycle LRCK for each audio data format is defined as Figure 73, Figure 74, Figure 75 and Figure 76. DAC output data can be selected by SDS [2:0] bits, as shown in Table 21.

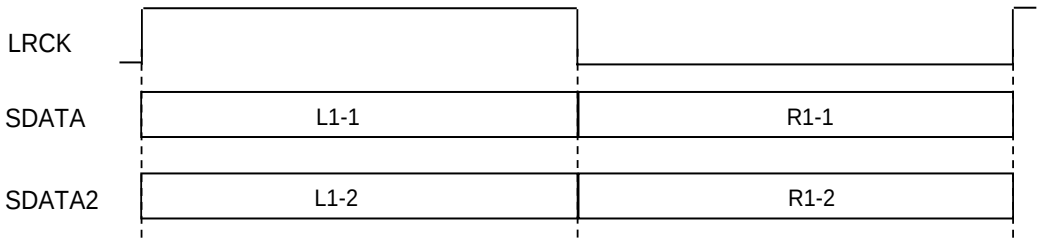


Figure 73. Data Slot in Normal Mode

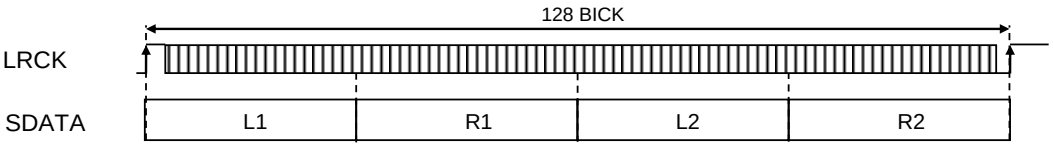


Figure 74. Data Slot in TDM128 Mode

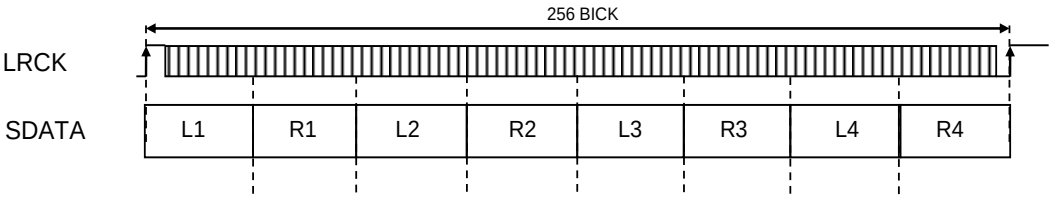


Figure 75. Data Slot in TDM256 Mode

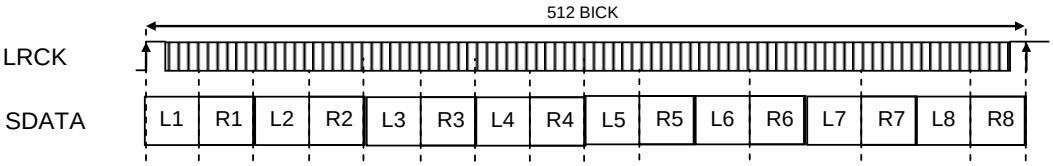


Figure 76. Data Slot in TDM512 Mode

Table 21. Data Select (×: Do not care)

	TDM [1:0] bits	SDS [2:0] bits	Lch	Rch
Normal Mode	00	×××	L1	R1
TDM128 Mode	01	××0	L1	R1
		××1	L2	R2
TDM256 Mode	10	×00	L1	R1
		×01	L2	R2
		×10	L3	R3
		×11	L4	R4
TDM512 Mode	11	000	L1	R1
		001	L2	R2
		010	L3	R3
		011	L4	R4
		100	L5	R5
		101	L6	R6
		110	L7	R7
		111	L8	R8

9.3.2. DSD Mode

Stereo Data is shifted in via the DSDL and DSDR pins using DCLK inputs (Figure 77). DSD data is supported by both Normal mode and Phase Modulation mode (Figure 78). The AK4191 does not support phase modulation when DSD512 and DSD1024 mode (DSDSEL [2:0] bits = “011” or “1××” when ADPE bit = ”0”, ADSDS [2:0] bits = “011” or “100” when ADPE bit = ”1”).

Polarity of DCLK is possible to invert by DCKB bit. Input data is clocked in on a rising edge of DCLK when DCKB bit = “0” and it is clocked in on a falling edge of DCLK when DCKB bit = “1”.
In case of DSD mode, the setting of DIF [2:0] bits are ignored.

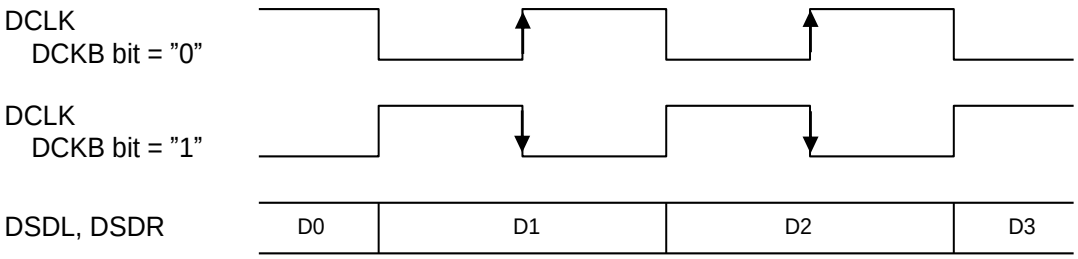


Figure 77. DSD Mode Timing

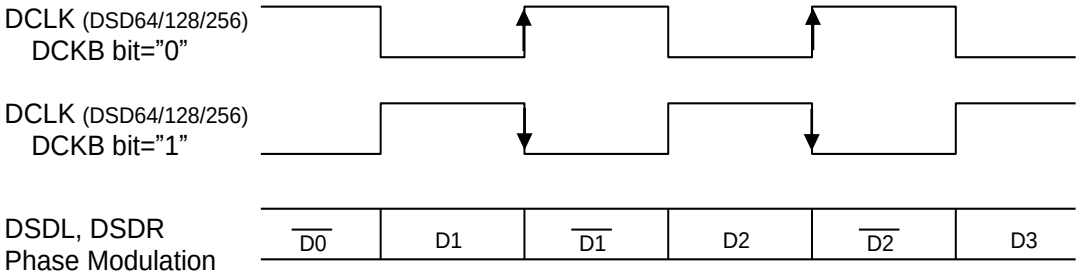


Figure 78. DSD Mode Timing (Phase Modulation Format)

9.3.3. External Digital Filter Mode (EXDF Mode)

The audio data is input by BCK and WCK from the DINL/L2 and DINR/R2 pins. Three formats are available (Table 22) by DIF [2:0] bits and DUAL bit setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must not burst. Mode 1 can be used for 16-bit and 32-bit, Mode 2 can be used for 16-bit, 24-bit, 32-bit and 48-bit by zeroing the unused LSBs.

Table 22. Audio Interface Format (EXDF Mode) (N/A: Not available)

Mode	DIF [2:0] bits	Input Format		
		DUAL bit = “0”	DUAL bit = “1”	
0	000	16-bit LSB justified	32-bit LSB justified	
-	001	N/A	N/A	
0	010	16-bit LSB justified	32-bit LSB justified	
-	011	N/A	N/A	
1	100	24-bit LSB justified	48-bit LSB justified	
2	101	32-bit LSB justified	64-bit LSB justified	
1	110	24-bit LSB justified	48-bit LSB justified	(default)
2	111	32-bit LSB justified	64-bit LSB justified	

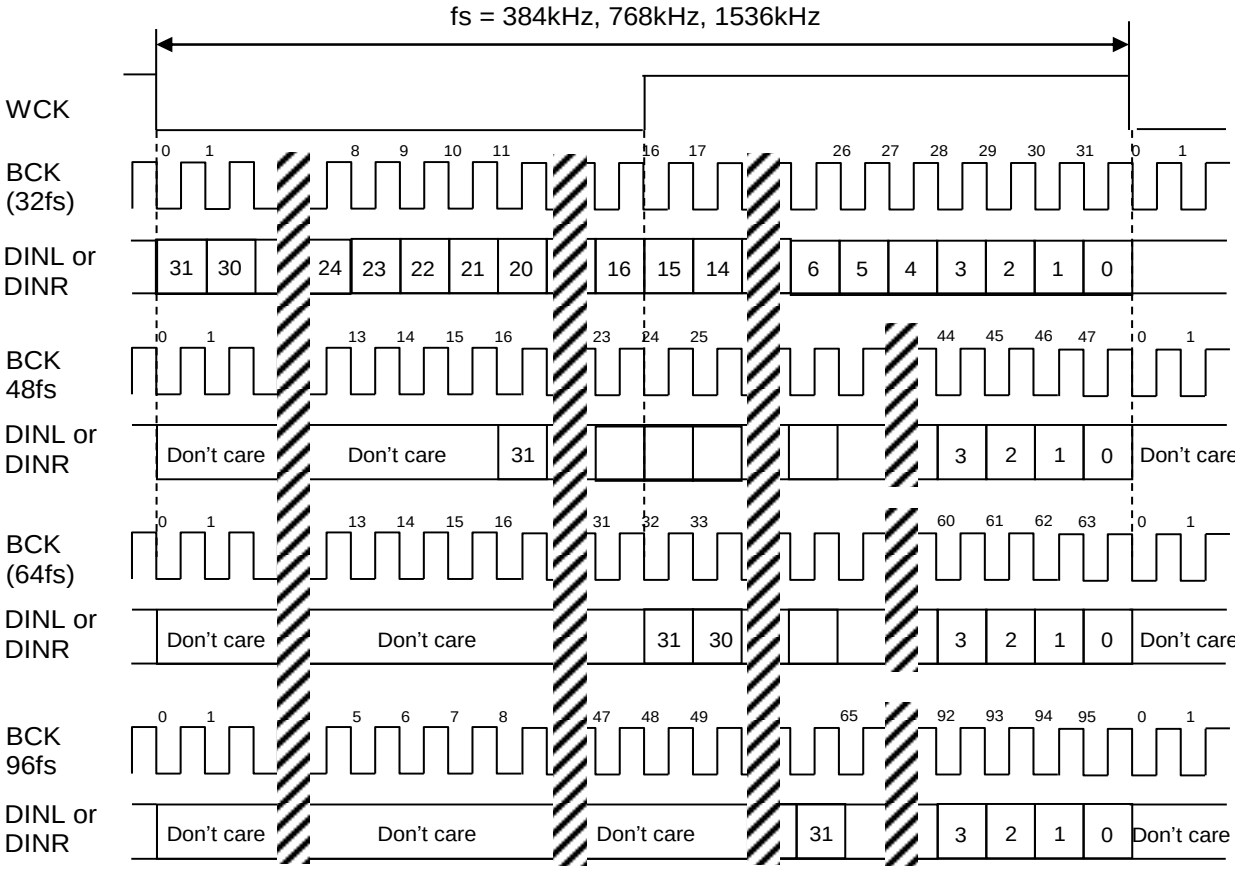


Figure 79. EXDF Mode Timing (DUAL bit = ”0”, 16/24/32-bit LSB justified)

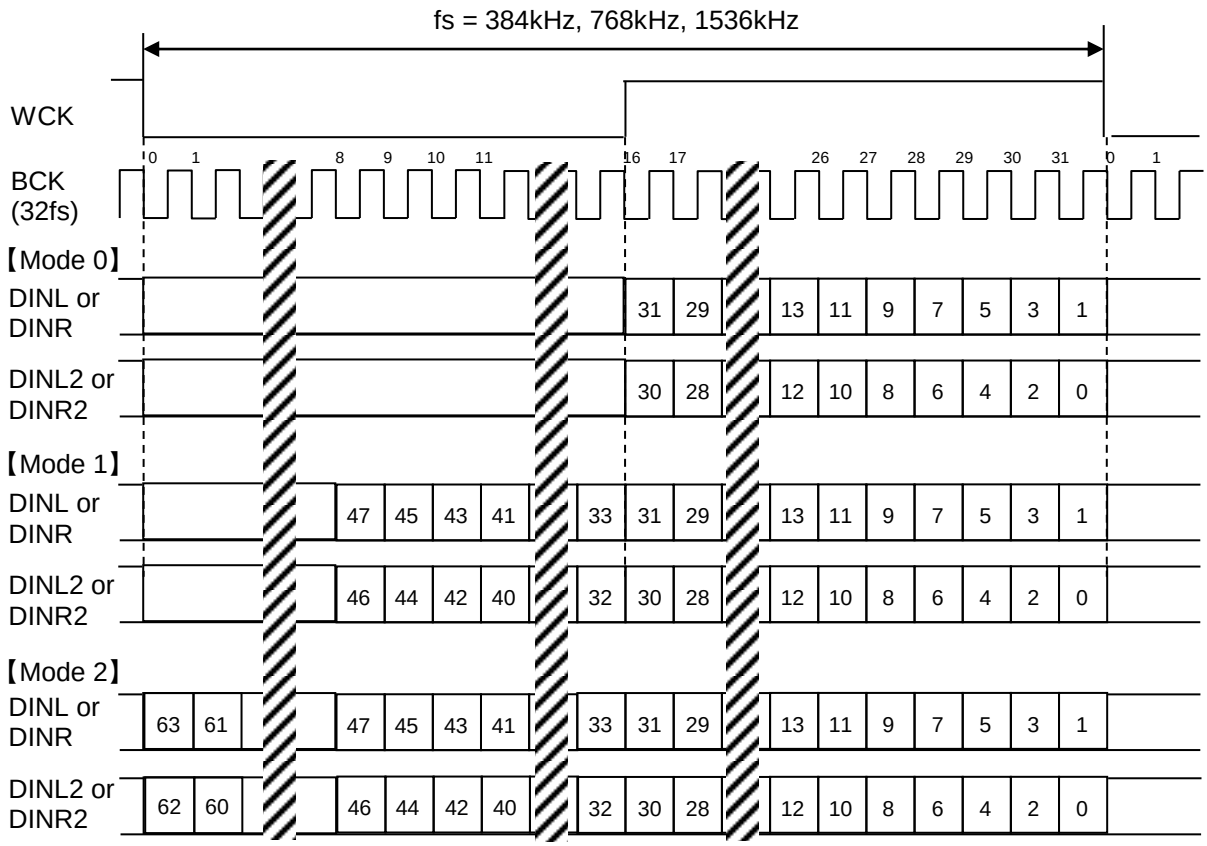


Figure 80. EXDF Mode Timing (DUAL bit =”1”, 32/48/64-bit LSB justified)

9.3.4. Delta Sigma Modulator Data Output (MBD7-1) Format

9.3.4.1. Multi-Bit Mono Interface mode (single channel mode, no adding) (OSTME bit = ”0”)

In this mode, AK4191 transmits one channel audio data. D0[7:1], D1[7:1], D2[7:1] and D3[7:1] are one channel data. Data is output to the MBD7-1 pins, respectively by synchronizing to BCKO. Data is clocked out on the falling edges of BCKO. When the output data bit length is six by setting OBIT [1:0] bit =”01”, MBD1 pin output becomes “L”. When the output data bit length is five by setting OBIT [1:0] bit =”10” or “11”, MBD1-2 pins output become “L”.

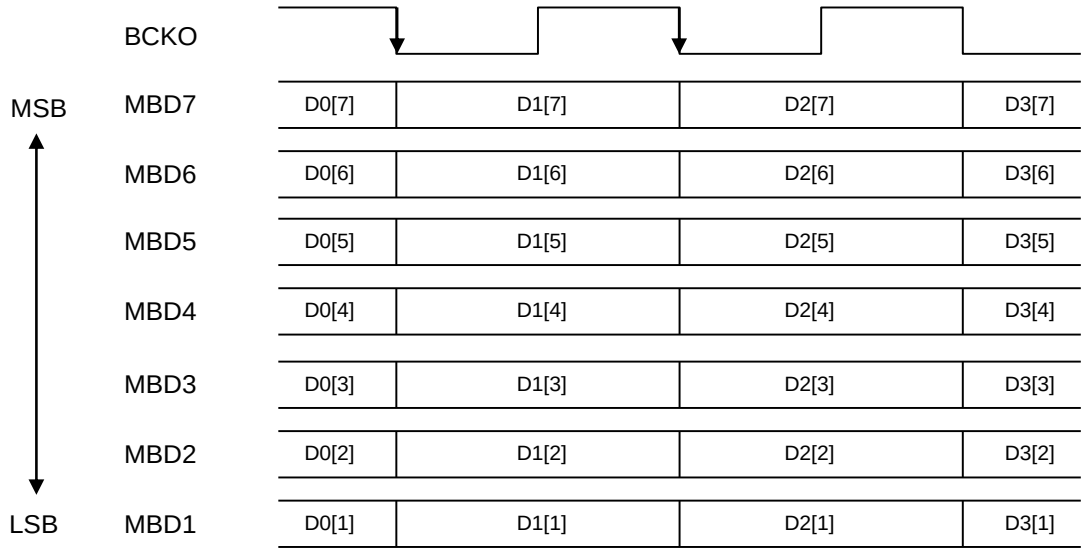


Figure 81. Multi-Bit Mono Interface mode

9.3.4.2. Multi-Bit Stereo Interface Mode (OSTME bit = “1”)

In this mode, AK4191 transmits Stereo channel audio data. R0[7:1], L1[7:1], R1[7:1], L2[7:1], R2[7:1] and L3[7:1] are stereo channel data. Data is output to the MBD7-1 pins, respectively by synchronizing to BCKO. Data is clocked out on both edges of BCKO. When the output data bit length is six by setting OBIT [1:0] bit =”01”, MBD1 pin output becomes “L”. When the output data bit length is five by setting OBIT [1:0] bit =”10” or “11”, MBD1-2 pins output become “L”.

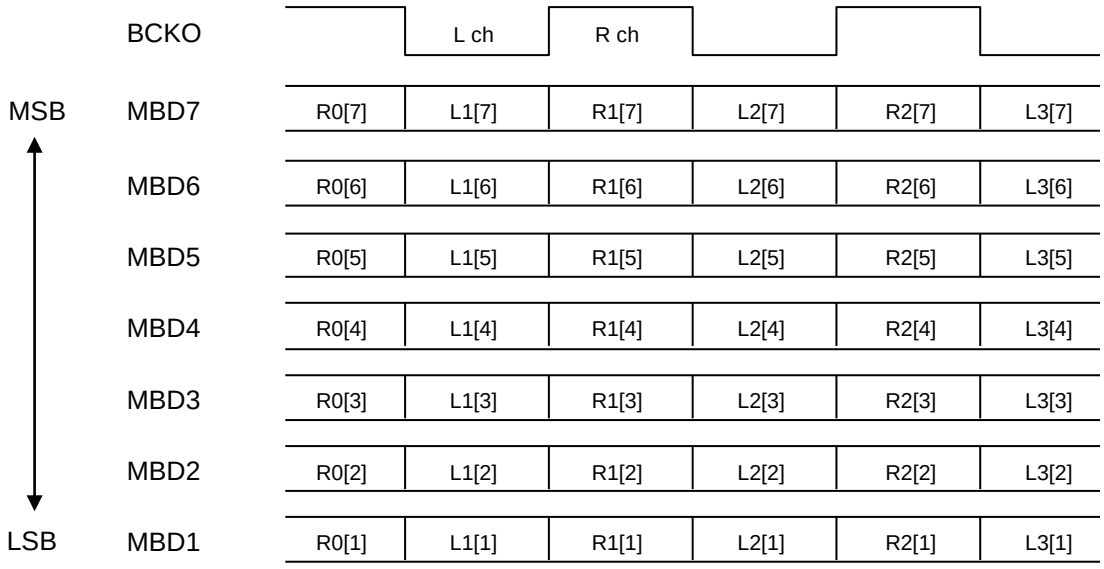


Figure 82. Multi-Bit I/F mode (Stereo mode)

9.3.5. Delta Sigma Modulator Data Input (DSMI7-1) Format

The AK4191 supports two modes, such as mono mode or stereo mode. Input data bit length is selectable by setting IBIT bit. When the input data bit length is six by setting IBIT bit =”1”, data must be input to the DSMI7-2 pins and DSMI1 pin must be "L". When the input data bit length is seven by setting IBIT bit =”0”, data must be input to the DSMI7-1 pins.

9.3.5.1. Multi-Bit Mono Interface mode (single channel mode, no adding) (ISTME bit = ”0”)

In this mode, AK4191 receives one channel audio data. D0[7:1], D1[7:1], D2[7:1] and D3[7:1] are one channel data. Data must be input respectively by synchronizing to BCKI. Data is clocked in on the rise edge of BCKI.

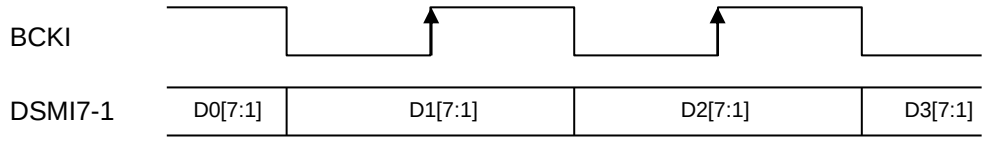


Figure 83. Multi-Bit Mono Interface mode

9.3.5.2. Multi-Bit Stereo Interface Mode (ISTME bit = “1”)

In this mode, AK4191 receives Stereo channel audio data. R0[7:1], L1[7:1], R1[7:1], L2[7:1], R2[7:1] and L3[7:1] are stereo channel data. Data must be input respectively by synchronizing to BCKI. Data is clocked in on both edge of BCKI. When the output bit number is six by setting IBIT bit =”1”, DSMI1 pin must be “L”.

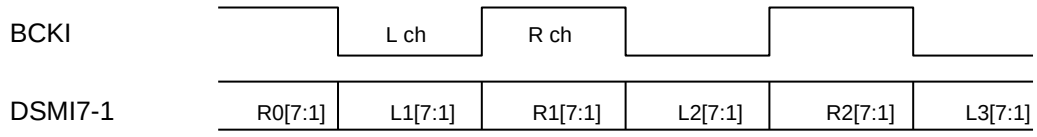


Figure 84. Multi-Bit I/F mode (Stereo mode)

9.4. Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4191 for sound color selection of music playback.

9.4.1. PCM Mode

9.4.1.1. Filter Selection

In PCM mode, the digital filter can be selected by the SD, SLOW and SSLOW bits (Table 23).

Table 23. Digital Filter Setting (N/A: not available)

SSLOW	SD	SLOW	Digital Filter Mode	
			1×/2×/4×/8×/16× speed mode	32× speed mode
0	0	0	Sharp Roll-off filter	Sharp Roll-off filter (default)
0	0	1	Slow Roll-off filter	
0	1	0	Short Delay Sharp Roll-off filter	
0	1	1	Short Delay Slow Roll-off filter	
1	0	0	Super Slow Roll-off filter	
1	0	1	Super Slow Roll-off filter	
1	1	0	Low Dispersion Short Delay filter	
1	1	1	Programmable filter	

The AK4191 has a programmable digital filter. The coefficients should be stored before using.

9.4.2. DSD Mode

In DSD mode, the cutoff frequency of digital filter can be switched by OBIT [1:0] bits and DSDF bit. Table 24 shows the cutoff frequency @fsb = 44.1 kHz. As shown in Table 24, there are prohibited filter settings depending on OSR bit and OBIT [1:0] bits when DSDD bit =”1”.

Table 24. DSD Filter Select

DSD rate	Internal DSD Filter Cut Off Frequency @fsb = 44.1 kHz						
	DSDD bit = ”0”	DSDD bit = ”1”					
		OBIT [1:0] = ”00”		OBIT [1:0] = ”01”		OBIT [1:0] = ”10” “11”	
		DSDF bit = ”0”	DSDF bit = ”1”	DSDF bit = ”0”	DSDF bit = ”1”	DSDF bit = ”0”	DSDF bit = ”1”
DSD64	22kHz	37 kHz	65 kHz	39 kHz	76 kHz	39 kHz	78 kHz
DSD128”	45kHz	74 kHz	131 kHz	78 kHz	152 kHz	78 kHz	156 kHz
DSD256	89kHz	144 kHz	238 kHz	156 kHz	304 kHz	156 kHz (Note 24)	312 kHz
DSD512	179kHz	288 kHz (Note 24)	476 kHz (Note 24)	312 kHz (Note 24)	608 kHz (Note 24)	Not Available	624 kHz (Note 24)
DSD1024	358kHz	Not Available		Not Available		Not Available	

Note 24. This mode is not available when OSR bit = “1”.

9.5. De-emphasis Filter (PCM Mode)

The AK4191 has a de-emphasis function by IIR filter (50/15 μsec). This function is only valid in PCM 1×/2×/4× speed mode and is disabled when using Super Slow Roll-off filter.

A digital de-emphasis filter is available for 32kHz, 44.1 kHz or 48 kHz sampling rates (tc = 50/15μsec) and is enabled or disabled by DEM [1:0] bits (Table 25). DEM [1:0] bits setting value is held even if the data mode is switched among PCM, DSD and EXDF modes.

Table 25. De-emphasis Control

DEM [1:0] bits	Mode	
00	44.1 kHz	
01	OFF	(default)
10	48 kHz	
11	32 kHz	

9.6. Digital Attenuator

The AK4191 includes a channel independent digital attenuator for output volumes (ATT) with 256 levels at 0.5dB step including MUTE (Table 26). When changing output levels, it is executed in soft transition, thus no switching noise occurs during these transitions. It can attenuate the input data from 0dB to –127dB and MUTE when assuming the output signal level is 0dB when ATTL [7:0] bits and ATTR [7:0] bits = "FFH".

The digital attenuator is disabled in volume bypass mode (DSDD bit = "1") at DSD mode. Digital attenuation is fixed to 0 dB in pin control mode.

Table 26. Attenuation Level of Digital Attenuator

ATTL/R [7:0] bits	ATT Code	Attenuation Level	
FFH	255	0dB	(default)
FEH	254	–0.5dB	
FDH	253	–1.0dB	
:	:	:	
:	:	:	
02H	2	–126.5dB	
01H	1	–127.0dB	
00H	0	MUTE (-∞)	

The transition time of when changing digital output volume is defined as (Transition time of 1 code shift) × (previous ATT level – changed ATT level). The transition time from setting 0dB to MUTE is set by ATS [1:0] bits (Table 27). Register setting values will be kept even switching the PCM and DSD modes.

Table 27. Transition Time between Set Values of ATTL/R[7:0] bits (fsb: Base Sampling Frequency)

ATS [1:0] bits	Transition time from setting 0dB to MUTE		
	specification	fsb = 44.1 kHz	
00	4080 / fsb	92.5msec	(default)
01	2040 / fsb	46.3msec	
10	510 / fsb	11.6msec	
11	255 / fsb	5.8msec	

It takes 4080/fsb (92.5 msec @fsb = 44.1 kHz) from "FFH" (0dB) to "00H" (MUTE) when ATS [1:0] bits "00" in PCM mode. ATTL [7:0] bits and ATTR [7:0] bits are initialized to "FFH" (0dB) by setting the PDN pin = "L".
If the digital volume attenuation level is changed during reset period, the output volume will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 10/fs after releasing reset.

9.7. Gain Adjustment Function

The AK4191 has the gain adjustment function. The digital output signal level can be adjusted by GC [3:0] bits (Table 28).

Table 28. Output Level between Set Values of GC [3:0] bits (×: Do Not Care)

GC [3:0]	Output Level			
	PCM	DSD: Normal Path	DSD: Volume Bypass	
0000	56%	56%	50%	(default)
0001	56%	50%	50%	
0010	62%	62%	50%	
0011	62%	50%	50%	
0100	75%	75%	50%	
0101	75%	50%	50%	
0110	80%	80%	50%	
0111	80%	50%	50%	
1xxx	50%	50%	50%	

This reference Output level is input signal, input signal is 100%.

There are prohibited gain settings depends on Delta-Sigma option settings shown in Table 46. Pop noise may occur if GC [3:0] bits are set prohibited setting.
As shown in Figure 85, Gain is adjusted before DSMI mix function.

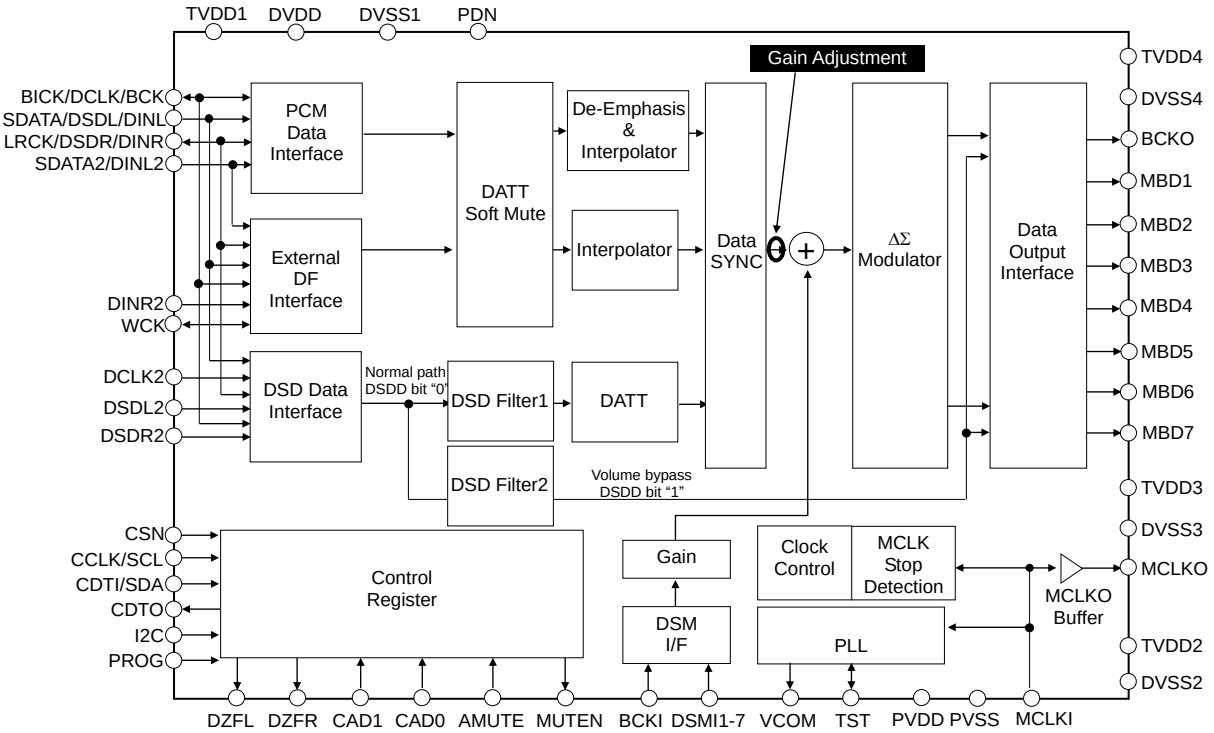


Figure 85. Gain Adjustment point

9.8. Zero Detection, DSD Full-scale Detection

The AK4191 has a zero detection function and a DSD full-scale detection function. These detection flags can be output from the DZFL/R pin. DDMOE, DZFE and DZFM bits select the output detection flag of the DZFL/R pin (Table 29). The output polarity of the DZFL/R pin can be inverted by DZFB bit (Table 30).

Table 29. Output Select for DZFL/R Pins (×: Do Not Care)

DDMOE bit	DZFE bit	DZFM bit	Output Detection Flag	DZFL Pin Output	DZFR Pin Output	
0	0	×	Disable	(output polarity is shown in Table 30.)		(default)
	1	0	Zero Detection Flag (DZF)	Lch DZF	Rch DZF	
		1		AND Signal of Lch and Rch DZF		
1	×	0	DSD Full-scale Detection Flag (DSDFF)	Lch DSDFF	Rch DSDFF	
	0	1		OR Signal of Lch and Rch DSDFF		
	1	1	Both DZF and DSDFF	AND Signal of Lch and Rch DZF	OR Signal of Lch and Rch DSDFF	

Table 30. Output Polarity Select for DZFL/R Pins

DZFB bit	DZFL/R Pin Output	
0	"H" when detect flag	(default)
1	"L" when detect flag	

9.8.1. Zero Detection Function

The AK4191 has a channel-independent zero detection function. As shown in Figure 86, DATT soft mute block outputs are the monitor nodes of zero detection. Zero detection flag is generated when the monitor node of each channel is continuously "0" for a detection time shown in Table 31.

Zero detection flag is generated immediately when the AK4191 is set to reset state (RSTN bit = "0"). Zero detection flag will be cleared in 5/fs-6/fs by releasing the reset (RSTN bit = "1").

Table 31. Zero Detection Time

Operation mode	Detection Time	@ MCLK Frequency = 11.2896MHz
PCM	4096 × 256 / Base MCLK Frequency	92.88 msec
EXDF		
DSD		

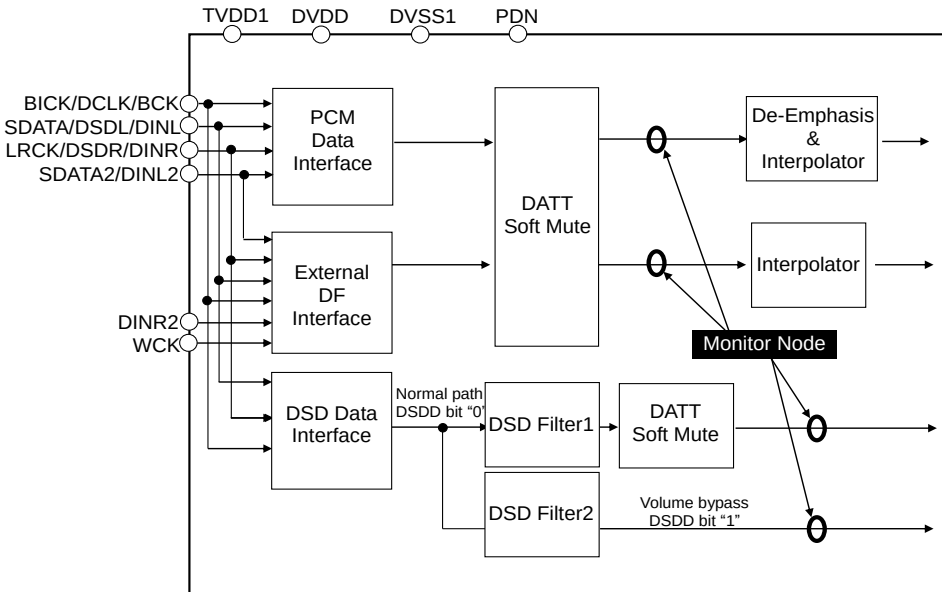


Figure 86. Zero Detection Monitor Node

9.8.2. DSD Full-Scale Detection Function

The AK4191 has independent full-scale detection function for each channel in DSD mode. Figure 87 shows a block diagram of DSD signal playback. Input data of each channel pin (DSDL or DSDR) is received via the DSD_IF block and full-scale detection is executed at the DSD full-scale detection block. Full-scale detection is valid only the AK4191 is in power-on state.

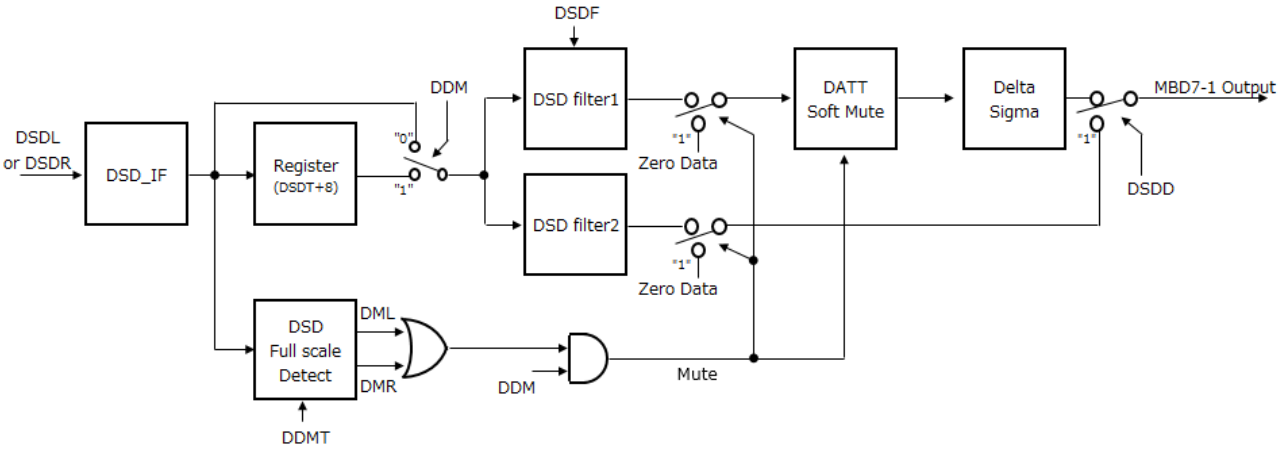


Figure 87. DSD Block Diagram

If the input data of any channel is continuously “H” or “L” for the time set by DDMT bit, the AK4191 is in full-scale detection state (Table 32) and corresponding DML or DMR bit becomes “1” independently. DML and DMR bits can be readout by register reading.

The AK4191 mutes the digital output after detecting full-scale signal if DDM bit = “1”. The output data of DSD_IF block is delayed by Register block for “Setting Time of DDMT bit + 8 DCLK cycles” to avoid clicking noise until the analog output is muted completely when DDM bit = “1”. Therefore, the digital output delay becomes larger according to this delay time (Table 32). DDM bit setting should be made while PMPLL bit = “0” or RSTN bit = “0”.

Full-scale detection state is released when the input data of the full-scale input channel is toggled. The operation after full-scale detection is released is according to DSDD bit setting that selects DSD playback path (Table 33).
When DSDD bit = “0” (Normal Path), the transition time until the output data returns to normal after releasing full-scale detection state is according to the setting of ATS [1:0] bits (Table 27).
If DSDD bit = “1” (Volume Bypass), the output data returns to normal immediately when the full-scale detection state is released.

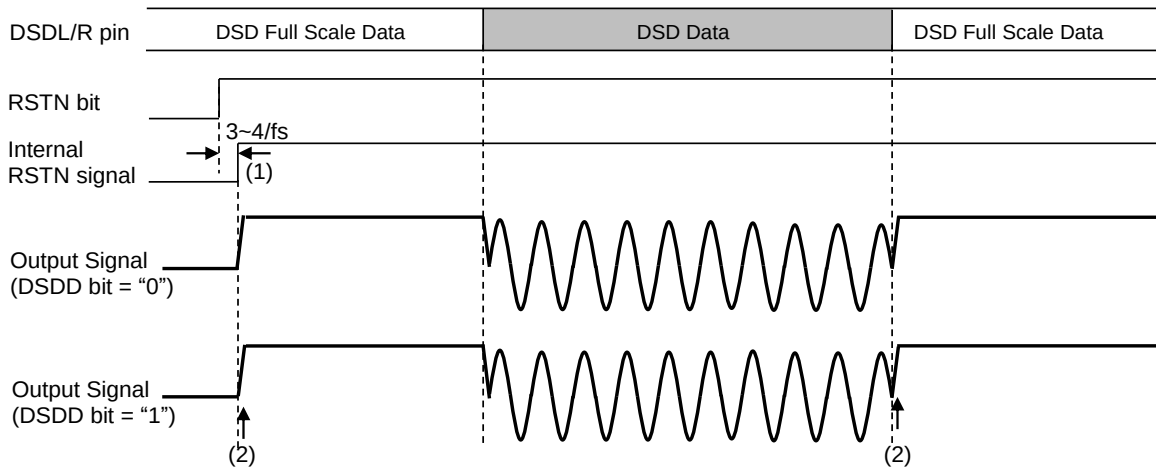
The full-scale detection function is assuming full-scale input that occurs when switching the data mode between PCM and DSD modes. Therefore, pop noise will not occur when the input signal becomes full-scale from zero data and vice versa but there is a possibility that pop noise occurs when the input signal becomes full-scale from the state there is an input signal and vice versa.

Table 32. DSD Full-scale Detection Time Setting

DDMT bit	Detection Time	Register Delay	
0	512 DCLK cycle	520 DCLK cycle	(default)
1	256 DCLK cycle	264 DCLK cycle	

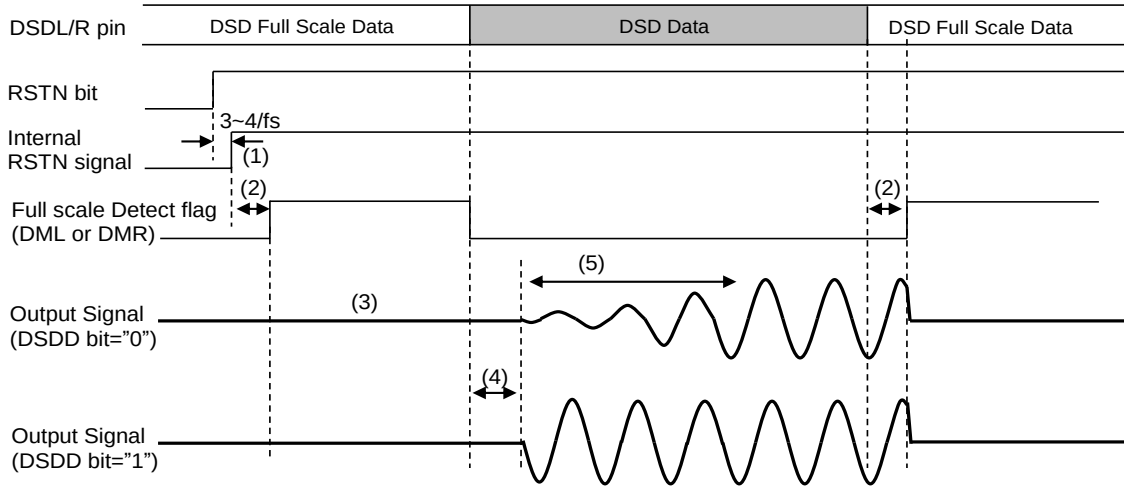
Table 33. Relationship between Output Signal Transition Time and DSDD Bit (DDM bit = “1”)

DSDD bit	Mode	Mute Transition time	Mute Release time	
0	Normal Path	Rapidly	As ATS [1:0] bits	(default)
1	Volume Bypass	Rapidly		



Notes:
(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".
(2) Excessive signals will be output from the analog output if full-scale signal is input after releasing internal reset. This behavior does not depend on DSDD bit setting.

Figure 88. Output Signal with DSD Full-scale Input (DDM bit = "0")



Notes:
(1) Internal reset is released after 3-4/fs by setting RSTN bit = "1".
(2) The internal detection flag becomes "1" if the input data is full-scale for a period set by DDMT bit after releasing internal reset.
(3) Analog output is forced to zero output when full-scale signal is detected. No clicking noise occurs during a period from digital data input until full-scale detection since the analog output data delays for Register delay time (Table 32) if DDM bit is set to "1".
(4) Full-scale detection state is cleared when normal signal is input when the AK4191 is in full-scale detection state. Analog signal output starts after the Register delay time (Table 32) by clearing the full-scale detection state.
(5) Analog output transition time is different according to DSDD bit setting. When DSDD bit = "0", analog output transition time is set by ATS[1:0] bits (Table 27). When DSDD bit = "1", analog output recovers immediately.

Figure 89. Output Signal with DSD Full-scale Input (DDM bit = "1")

9.9. LR Channel Output Signal Select, Phase Inversion Function

Input and output combination of the AK4191 can be changed by MONO bit and SELLR bit. In addition, the output signal phase can be inverted by INVL bit and INVR bit (Table 34). These functions are available on all audio formats.

Table 34. Output Select

MONO bit	SELLR bit	INVL bit	INVR bit	OSTME bit ="0"	OSTME bit ="1"	
				MBD output	MBD Lch output	MBD Rch output
0	0	0	0	Lch in	Lch in	Rch in
		1	0	Lch in Invert	Lch in Invert	Rch in
		0	1	Lch in	Lch in	Rch in Invert
		1	1	Lch in Invert	Lch in Invert	Rch in Invert
0	1	0	0	Rch in	Rch in	Lch in
		1	0	Rch in Invert	Rch in Invert	Lch in
		0	1	Rch in	Rch in	Lch in Invert
		1	1	Rch in Invert	Rch in Invert	Lch in Invert
1	0	0	0	Lch in	Lch in	Lch in
		1	0	Lch in Invert	Lch in Invert	Lch in
		0	1	Lch in	Lch in	Lch in Invert
		1	1	Lch in Invert	Lch in Invert	Lch in Invert
1	1	0	0	Rch in	Rch in	Rch in
		1	0	Rch in Invert	Rch in Invert	Rch in
		0	1	Rch in	Rch in	Rch in Invert
		1	1	Rch in Invert	Rch in Invert	Rch in Invert

9.10. Automatic Data Conversion Mode Switching

The AK4191 has automatic mode switching function that determines D/A conversion mode from the input clock and data. This function is available by setting ADPE bit = “1”. DP bit is for manual setting. It will be ignored when ADPE bit is “1”.

The automatic mode switching function is valid between PCM mode and DSD mode or EXDF mode and DSD mode. PCM/DSD automatic switching mode is enabled by setting ADPE bit = “1” when EXDF bit = “0”, EXDF/DSD automatic switching mode is enabled by setting ADPE bit = “1” when EXDF bit = “1”. EXDF bit setting should be made before changing ADPE bit = “0” → “1”. Note that automatic mode switching function is not available between PCM mode and EXDF mode.

The result of automatic mode detection can be readout by ADP bit. When ADPE bit = “1”, ADP bit outputs “0” if the detection result is PCM or EXDF mode and outputs “1” if it is DSD mode. This readout function of ADP bit is invalid and “0” data is readout when ADPE bit = “0”.

To judge PCM (or EXDF) mode or DSD mode correctly, the mute function of DSD full-scale detection should be enabled by setting DDM bit = “1” when using this automatic mode switching function. DDM bit must be set while PMPLL bit or RSTN bit = “0”. By setting DDM bit = “1”, group delay will be 36/fs longer in PCM/EXDF mode and 264 to 520 DCLK cycle longer according to full-scale detection time setting by DDMT bit in DSD mode (Table 32). This function does not support DSD phase modulation format and edge inversion function of DSD receiving data (DCKB bit = “1”).

The automatic mode switching function supports both DSD data paths set by DSDPATH bit. The AK4191 determines mode from the clock input of the DCLK2 pin (#10) when DSDPATH bit = “0”, and it determines mode from clock and data inputs of the BICK/BCK/DCLK pin (#2), LRCK/DSDR pin (#4) and WCK pin (#7).

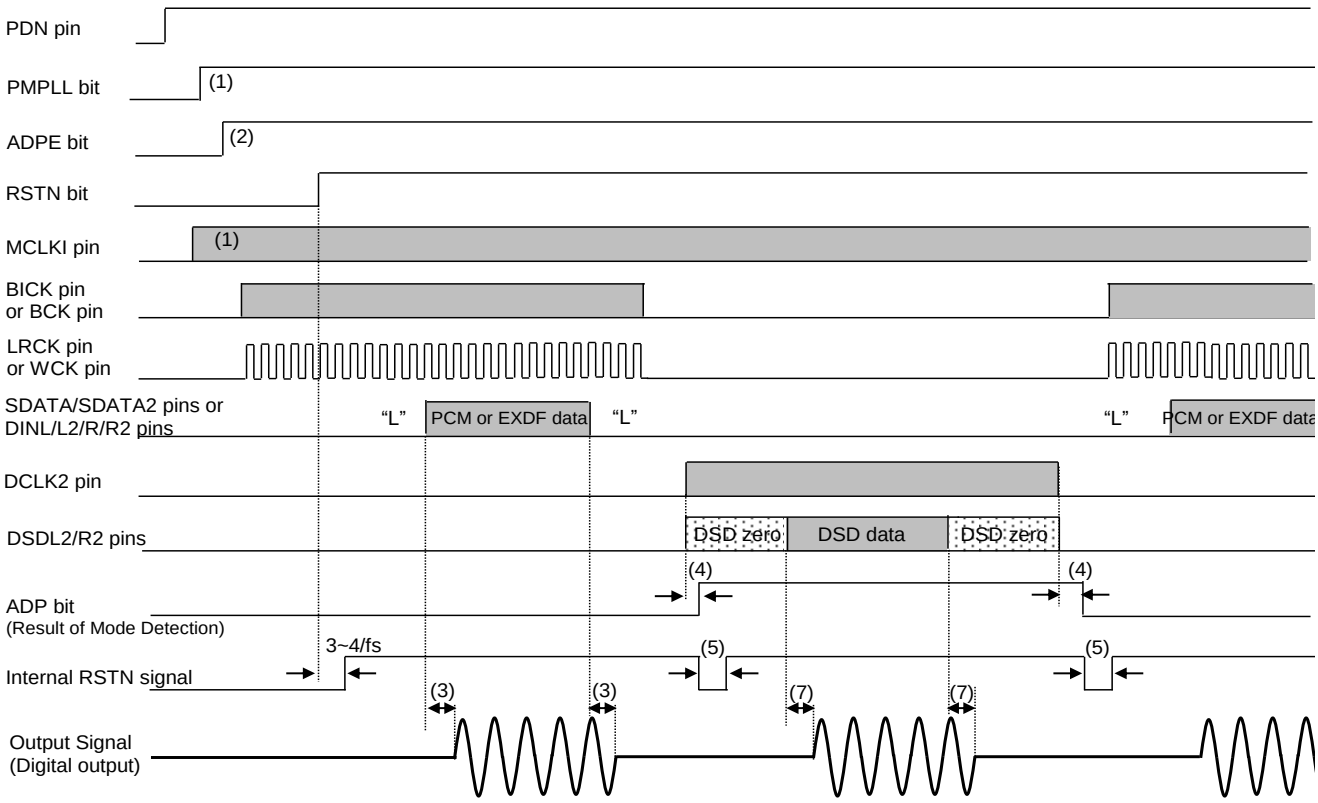
9.10.1. Mode Detection when DSD data and clock input to #2, #3, #4 pins. (DSDPATH bit = “0”)

When DSDPATH bit = “0”, the AK4191 judges PCM (or EXDF) mode or DSD mode by detecting a clock input to the DCLK2 pin (#10). MCLK should be input during mode detection.
The AK4191 detects DSD mode if the frequency of DCLK2 is in a range shown in Table 35 and PCM (or EXDF) mode is detected if not.

Table 35. Mode Detection Condition when DSDPATH = ”0”

DCLK2 Frequency Range [MHz]		Detection Result
44.1 kHz base	48 kHz base	
2.5 to 50	2.7 to 50	DSD Mode

The AK4191 executes internal reset for 5/fsb-6/fsb automatically when switching the data mode and resumes operation. Refer to Figure 90 for operation sequence.



Notes:
(1) When DSDPATH bit = “0”, Internal master clock necessary for mode detection. MCLK should be input and Internal PLL reset should be released (PMPLL bit = “1”) before setting ADPE bit = ”1”.
(2) Automatic mode switching between PCM (or EXDF) and DSD modes is enabled by setting ADPE bit = “1”.
(3) In PCM mode, output delay time becomes longer for about 36/fs comparing with when setting ADPE bit = “0”.
(4) The AK4191 transitions to DSD mode if the frequency of DCLK2 satisfies the condition (Table 35).
(5) When data mode is changed, the AK4191 executes internal reset for 5/fsb-6/fsb automatically.
(6) In DSD mode, output delay time becomes longer comparing with when setting ADPE bit = “0”. In this case, delay time depends on DDMT bit setting.
(7) The AK4191 transitions to PCM (or EXDF) mode if the frequency of DCLK2 does not satisfy the condition.

Figure 90. Mode Switching Sequence when DSDPATH bit = “0”

9.10.2. Mode Detection when DSD data and clock input to #8, #9, #10 pins. (DSDPATH bit = "1")

When the DSDPATH bit = "1", the AK4191 detects PCM (or EXDF) mode or DSD mode from a clock and data inputs of the BICK/BCK/DCLK pin (#2), LRCK/DSDR pin (#4) and WCK pin (#7).

9.10.2.1. Mode Detection Start Condition

If one of the five conditions shown below is satisfied, the AK4191 executes mode detection. The AK4191 keeps previous mode instead of executing mode detection if any condition is not satisfied. These start conditions of mode detection are common regardless of DSDPATH bit and EXDF bit setting.

1. Input data of all channels are zero for a period set by ADPT [1:0] bits (Table 36).
2. Output data of all channels are zero for a period set by ADPT [1:0] bits (Table 36) because of the attenuation setting or SMUTE bit setting.
3. Input data of all channels are full-scale for a period set by DDMT bit in DSD mode (Table 32).
4. RSTN bit = "0"
5. Internal master Clock (PLLCK) is not stable.

Table 36. Time Until Mode Detection after Input Data Becomes Zero

ADPT [1:0] bits	Wait Time	
00	(4096 + 36) × 256 / Base MCLK Frequency	(default)
01	(2048 + 36) × 256 / Base MCLK Frequency	
10	(1024 + 36) × 256 / Base MCLK Frequency	
11	(8192 + 36) × 256 / Base MCLK Frequency	

9.10.2.2. PCM/DSD Mode Automatic Switching (EXDF bit = "0")

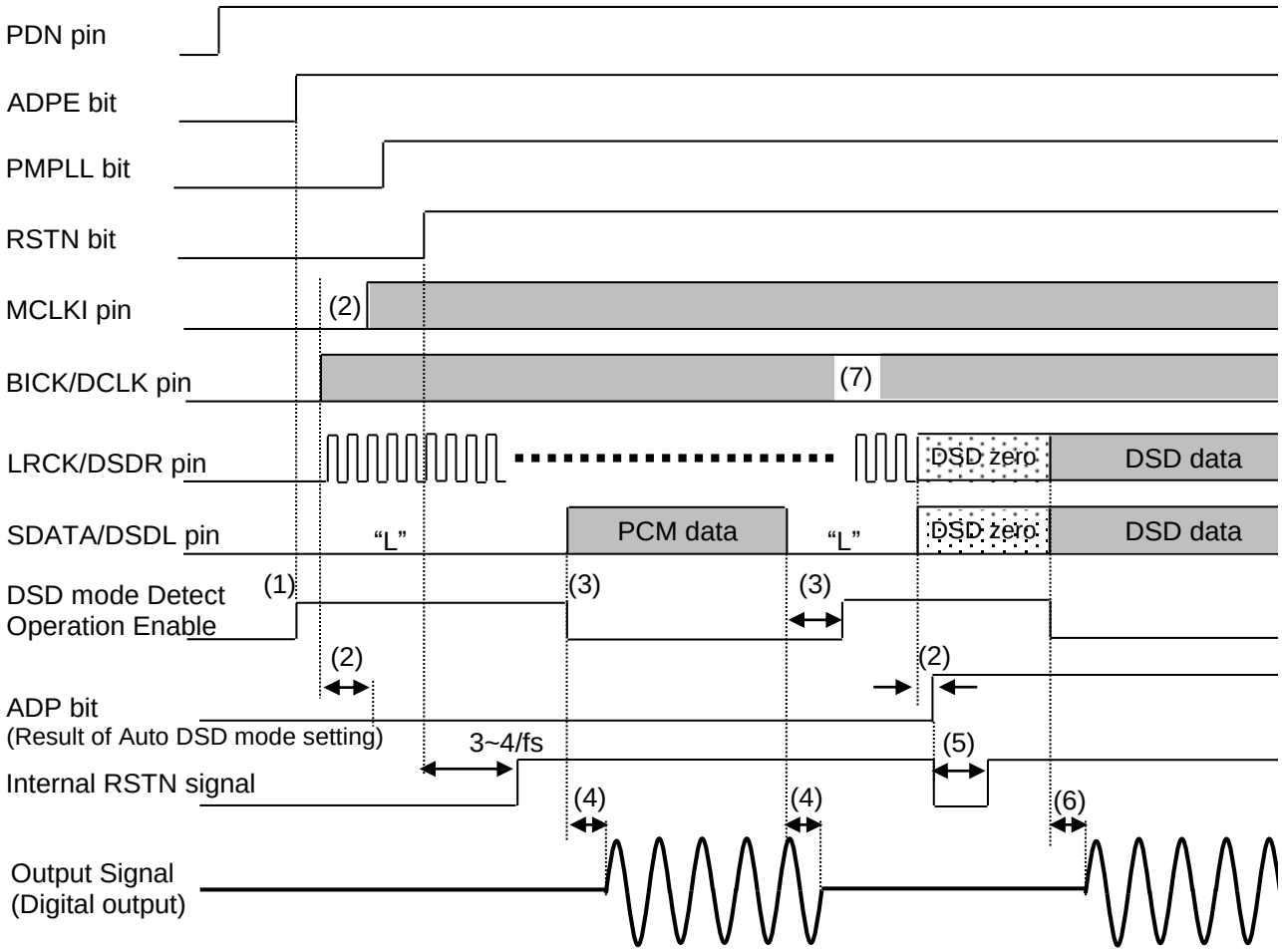
The AK4191 detects mode from the input signal to the LRCK/DSDR pin (#4). Input one of "01101001 01101001", "01010101 01010101", or "00110011 00110011" zero code pattern continuously to the LRCK/DSDR pin when changing to DSD mode from PCM mode (Table 37).

Input a clock that toggles in N times 16BICK cycle or a clock that is continuously "L" or "H" for 32BICK cycles or more to the LRCK/DSDR pin (#4) (Table 37). Refer to Figure 91 and Figure 92 for operation sequence.
The AK4191 keeps previous mode instead of executing mode switching if any condition is not satisfied.

Table 37. Input Signal when Switching PCM/DSD Mode

#4 LRCK/DSDR Pin Input Signal	Detection Result
One of zero code pattern below is input twice consecutively "01101001 01101001" or "01010101 01010101" or "00110011 00110011"	DSD Mode
Clock toggles in N times 16BICK cycles (N ≥ 1) or Clock that keeps "L" or "H" for 32BICK cycles	PCM Mode

The AK4191 executes data mode detection even if there is no MCLK input while RSTN bit = "0". However, the output becomes zero signal state ("L") and the AK4191 enters standby state when MCLKs stopped. The AK4191 resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/BCK/DCLK pin (#2) is stopped.
The AK4191 executes internal reset for 5/fsb-6/fsb automatically when switching the data mode and resumes operation.



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR pin. Mode detection is executed even when there is no MCLK input. The AK4191 starts data mode detection when input data of both channels are zero for a period set by ADPT [1:0] bits.

(3) The AK4191 finishes data mode detection when a data that is not zero is input.

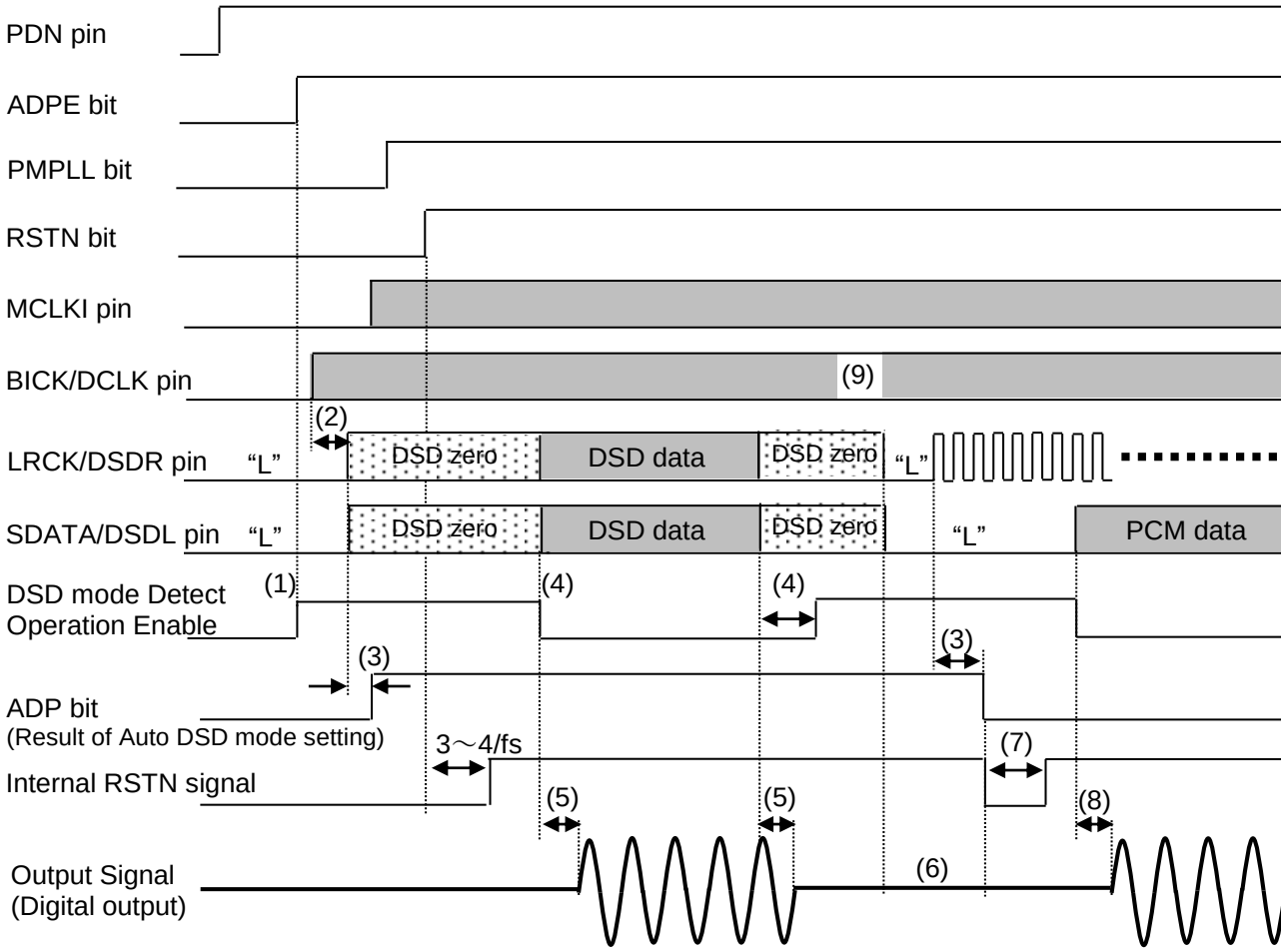
(4) In PCM mode, output delay time becomes 36/fs longer comparing with when setting ADPE bit = "0".

(5) When data mode is changed, the AK4191 executes internal reset for 5/fsb-6/fsb automatically.

(6) In DSD mode, output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(7) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 91. Changing to DSD Mode after Power-up in PCM Mode (DSDPATH bit = "1", EXDF bit = "0")



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting ADPE bit = "1" after setting the PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(2) Upon power up the AK4191, the AK4191 operates in PCM mode if DCLK is input and DSDL is not input.

(3) Mode detection is performed by monitoring input signal code pattern of the LRCK/DSDR pin. It is executed for 34 cycles of the BICK/DCLK pin input clock and then ADP bit is changed on a rising edge of input signal of the LRCK/DSDR pin. ADP bit outputs "0" in PCM mode and "1" in DSD mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4191 finishes data mode detection when a data that is not zero is input. Then the AK4191 restarts the mode detection when input data of all channels are continuously zero for the period set by ADPT [1:0] bits.

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) If DSD data input is stopped in DSD mode, the AK4191 stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4191. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

(7) When data mode is changed, the AK4191 executes internal reset for 5/fsb-6/fsb automatically.

(8) In PCM mode, output delay time becomes 36/fs longer comparing with when setting ADPE bit = "0".

(9) A clock input to the BICK/DSLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 92. Changing to PCM Mode after Power-up in DSD Mode (DSDPATH bit = "1", EXDF bit = "0")

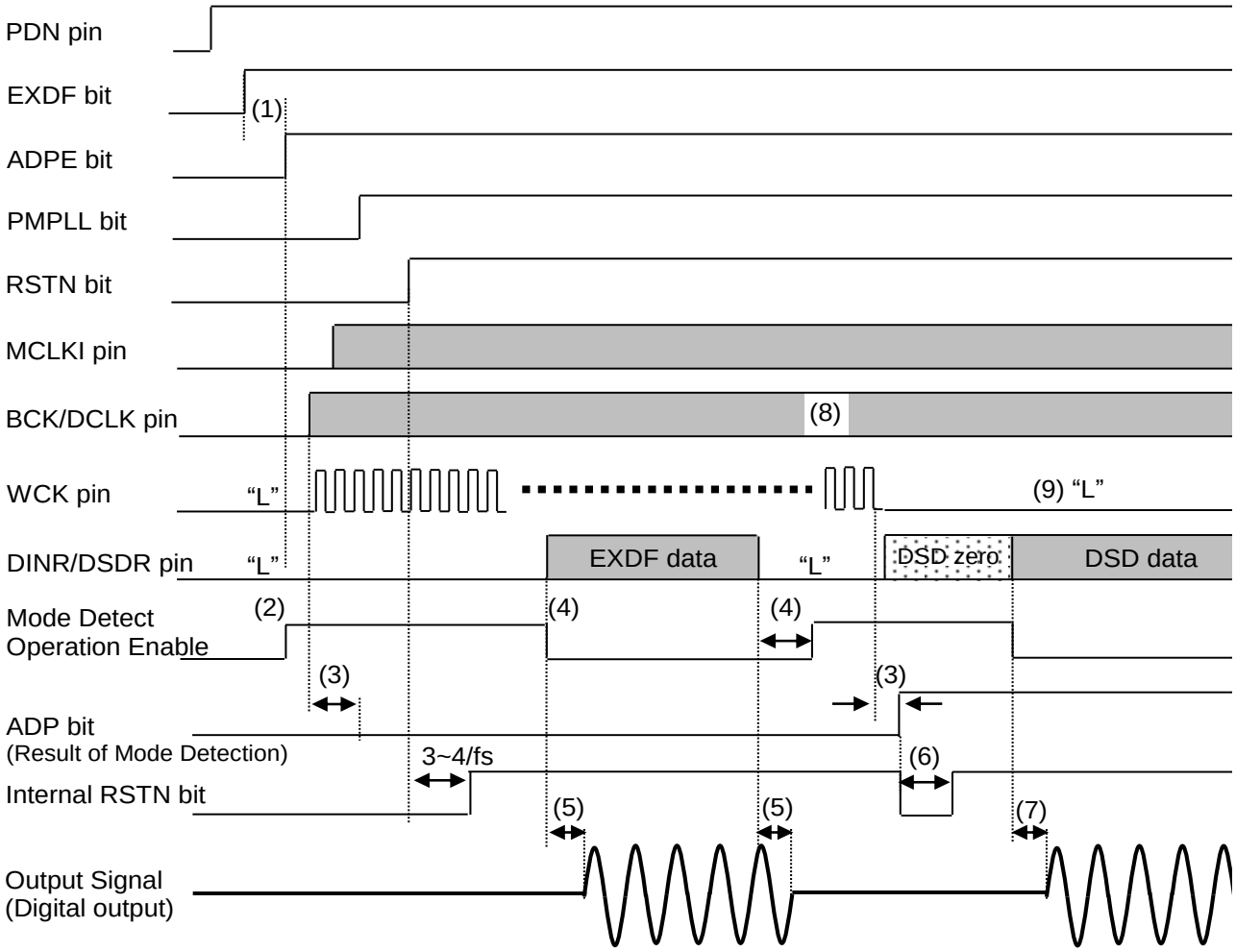
9.10.2.3. EXDF/DSD Automatic Mode Switching (EXDF bit = “1”)

The AK4191 detects mode from the input clocks to the WCK pin (#7) and the BCK/DCLK pin (#2). DSD mode is detected if the number of rising edge of the BCK/DCLK input clock exceeds 256 times in one cycle WCK input clock counting from a rising edge. EXDF mode is detected if the number of rising edge of the BCK/DCLK input clock does not reach 256 times in one cycle WCK input clock twice continuously (Table 38). Refer to Figure 93 and Figure 94 for the operation sequence.
The AK4191 keeps previous mode instead of executing mode switching if any condition is not satisfied.

Table 38. Mode Detection Conditions when Switching EXDF/DSD Mode

BCK/DCLK Pulse in One WCK Cycle	Detection Result
Once “256 < BCK/DCLK pulse number”	DSD Mode
Twice Continuously “BCK/DCLK pulse number ≤ 256”	EXDF Mode

The AK4191 executes data mode detection even if there is no MCLK input while PW bit = “0” or RSTN bit = “0”. However, the output becomes zero signal state (“L”) and the AK4191 enters standby state when MCLK is stopped. The AK4191 resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BCK/DCLK pin (#2) is stopped.
The AK4191 executes internal reset for 5/fsb-6/fsb automatically when switching the data mode and resumes operation.



Notes:

(1) EXDF bit must be set before setting ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring input clock of the WCK pin and the BCK/DCLK pin. It takes 256DCLK cycles for mode switching from EXDF to DSD mode and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4191 finishes data mode detection when a data that is not zero is input. The AK4191 restarts data mode detection when input data of both channels are zero for a period set by ADPT [1:0] bits.

(5) In EXDF mode, output delay time becomes 36/fs longer comparing with when setting ADPE bit = "0".

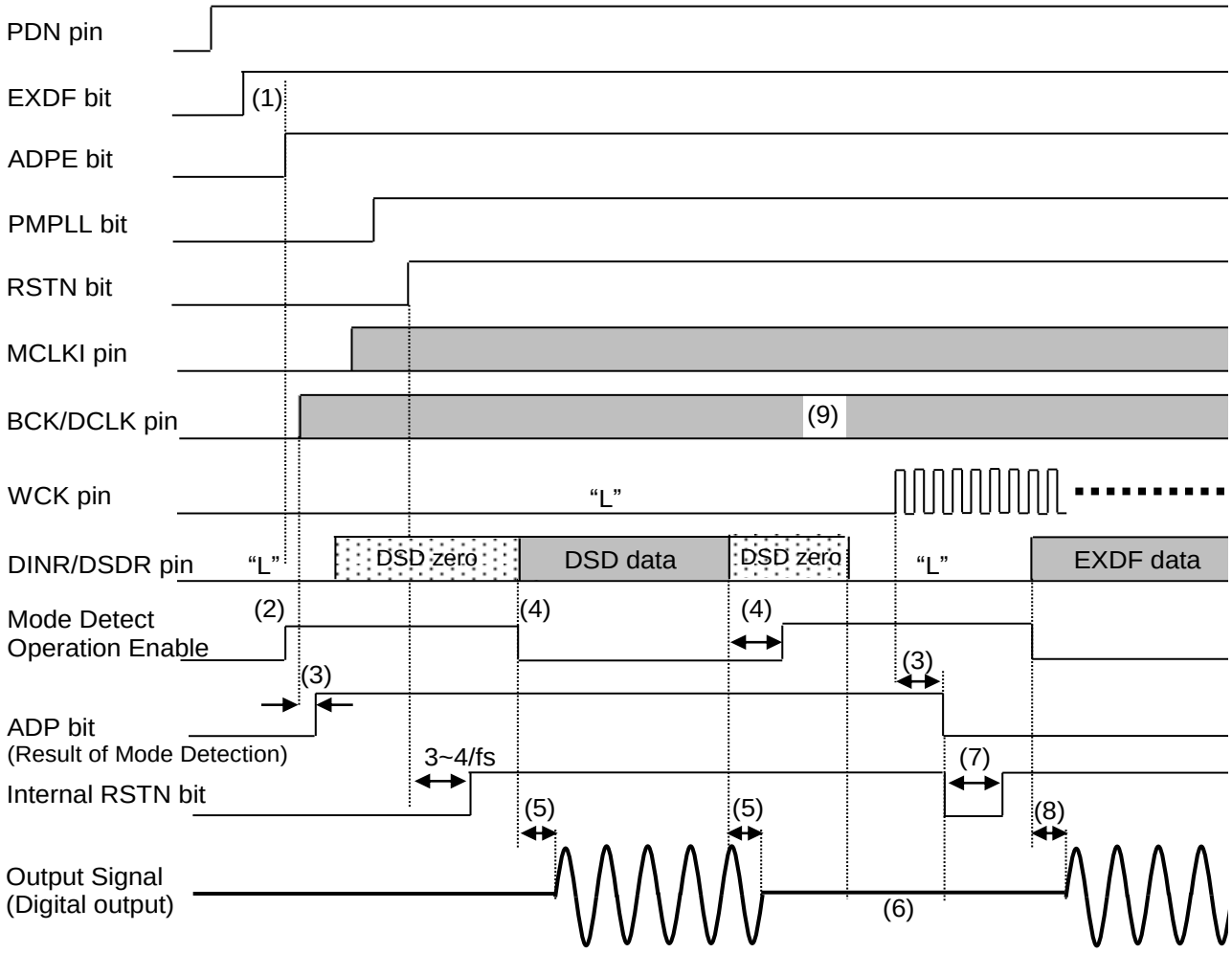
(6) When DSD mode is changed, the AK4191 executes internal reset for 3/fs to 4/fs automatically.

(7) In DSD mode, output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(8) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

(9) WCK input should be "L" when using DSD mode since DSD mode detection is performed by monitoring presence or absence of the WCK input clock when EXDF bit = "1".

Figure 93. Changing to DSD Mode after Power-up In EXDF Mode (DSDPATH bit = "1", EXDF bit = "1")



Notes:

(1) EXDF bit must be set before setting ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting ADPE bit = "1" after setting PDN pin "L" → "H". If RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring input clock of the WCK pin and the BCK/DCLK pin. It takes 256DCLK cycles for mode switching from EXDF to DSD mode and takes 2WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4191 finishes data mode detection when a data that is not zero is input. The AK4191 restarts data mode detection when input data of both channels are zero for a period set by ADPT [1:0] bits.

(5) In DSD mode, analog output delay time becomes longer comparing with when setting ADPE bit = "0". In this case, delay time depends on DDMT bit setting.

(6) If DSDR input is stopped in DSD mode, the AK4191 stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4191. Excessive signal output can be avoided by setting DDM bit = "1" enabling automatic mute function works when detecting DSD full-scale input.

(7) When data mode is changed, the AK4191 executes internal reset for 3/fs to 4/fs automatically.

(8) In EXDF mode, output delay time becomes 36/fs longer comparing with when setting ADPE bit = "0".

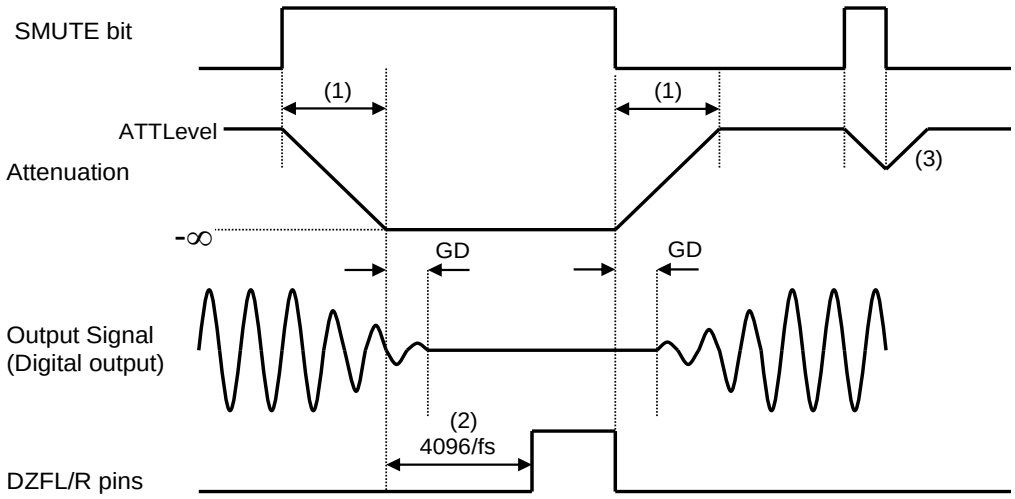
(9) A clock input to the BICK/DCLK pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK pin is stopped.

Figure 94. Changing to EXDF Mode after Power-up In DSD Mode (DSDPATH bit = "1", EXDF bit = "1")

9.11. Soft Mute Function

The AK4191 has soft mute function. The soft mute operation is performed at digital domain. When setting the SMUTE bit to “1”, the output signal is attenuated by −∞ during ATTDATA × ATT transition time from the current ATT level.
When setting back the SMUTE bit to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATTDATA × ATT transition time (Refer to Table 27 for ATT). If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

Soft mute function is not available when bypassing the volume (DSDD bit = “1”) in DSD mode.



Notes:
(1) ATTDATA × ATT transition time. For example, this time is 4080 / Base Sampling Frequency (fsb) at ATS [1:0] bits = “00”, ATTDATA = “FFH” in PCM 1× speed mode.
(2) When the input data for each channel is continuously zeros for 4096 × 256 / Base MCLK Frequency (92.8msec @Base MCLK Frequency fCLKb = 11.2896 MHz), the DZFL/R pin for each channel goes to “H”. The DZFL/R pin immediately returns to “L” if the input data is not zero.
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 95. Soft Mute Function

9.12. Mute signal output (MUTEN bit)

The AK4191 outputs MUTEN flag to inform internal state. Conditions MUTEN pin outputs “L” are selectable by using MUTES [1:0] bits (Table 39).

Table 39. Conditions for Output MUTEN pin = “L” (× : Do Not Care)

Conditions						MUTEN pin Output			
AMUTE pin	RSTN bit	Internal Master Clock	MCLK	Zero Data detection	DSD full-scale code detection	MUTES [1:0] bits setting			
						“00” (default)	01	10	11
H	×	×	×	×	×	L	L	L	L
L	0	×	×	×	×	L	L	L	L
	1	unstable	×	×	×	L	L	L	H
		×	Not supplied	×	×	L	L	L	H
		stable	supplied	detected	×	L	L	H	H
				Not detected	detected	L	H	H	H
					Not detected	H	H	H	H

9.13. Delta Sigma Modulator Data zero output

The AK4191 has data stop function. This function is enabled by setting MBDZ bit = ”1”. MBD7-1 pins go to “L” when MUTEN pin outputs “L”. Conditions MUTEN pin goes to “L” are shown in Table 39.

9.14. Delta Sigma Modulator Data Mix Function

The AK4191 has data mix function. This function is enabled by setting PMDSMI bit = “1”. Data input via DSMI1-7 pins with gain control function are added when setting SUBL/R bit = ”0” and are subtracted when setting SUBL/R bit = ”1” (Table 40).

Table 40. Data Mix function

PMDSMI	SUBL/R	Data Mix Function	
0	×	disable	(default)
1	0	Add DSMI data	
1	1	Sub DSMI data	

The gain of data can be controlled independently between channels by setting GAIN2L/R bits and ATTMXL/R [7:0] bits. When changing gain levels, it is executed in soft transition, thus no switching noise occurs during these transitions. The gain level is varied with 256 levels at 0.5dB step. The signal level is assumed 0dB when ATTMXL [7:0] bits and ATTMXR [7:0] bits = “FFH” and GAIN2L bit and GAIN2R bit are setting “0”. It can attenuate the data from 0dB to −127dB and MUTE when GAIN2L bit and GAIN2R bit are setting “0” and can attenuate the data from +6dB to −121dB and MUTE when GAIN2L bit and GAIN2R bit are setting “1” (Table 41).

Table 41. Gain Control Level of Data Mix Function

ATTMXL/R [7:0] bits	ATT Code	Gain Control Level		
		GAIN2L/R bit = ”0”	GAIN2L/R bit = ”1”	
FFH	255	0dB	+6dB	
FEH	254	−0.5dB	+5.5dB	
FDH	253	−1.0dB	+5.0dB	
:	:	:	:	
:	:	:	:	
02H	2	−126.5dB	−120.5dB	
01H	1	−127.0dB	−121.0dB	
00H	0	MUTE (-∞)	MUTE (-∞)	(default)

The transition time from setting 0dB to MUTE is set by ATSMX [1:0] bits (Table 42).

Table 42. Transition Time between Set Values of ATTMXL/R [7:0] bits

ATSMX [1:0] bits	Transition Time from setting 0dB to MUTE	
00	4080 × 256 / Base MCLK Frequency	(default)
01	2040 × 256 / Base MCLK Frequency	
10	510 × 256 / Base MCLK Frequency	
11	255 × 256 / Base MCLK Frequency	

It takes 4080 × 256 / Base MCLK Frequency (92.5 msec @Base MCLK Frequency = 11.2896 MHz) from “FFH” (0dB) to “00H” (MUTE) when ATSMX [1:0] bits “00”. ATTMXL [7:0] bits and ATTMXR [7:0] bits are initialized to “FFH” (0dB) by setting the PDN pin = “L”.
If the gain control level is changed during reset period, the gain level will become a setting value after releasing the reset. It will change to a setting value immediately if the volume is changed within 10/(256/Base MCLK Frequency) after releasing reset.

9.15. Master Clock output (MCLKO)

The AK4191 has a clock output function to operate Analog-DAC. When MCKOE bit = “1”, the clock generated from a clock input via MCLKI pin is output to MCLKO pin. The MCLKI and MCLKO frequency ratio is selectable by setting MCKDV bit.

Table 43. MCLKO output and MCLKI input frequency (fCLK) (×: do not care)

PDN pin	MCKOE bit	MCKDV bit	MCLKO output	
			state	Frequency
L	×	×	“L”	0
H	0	×	“L”	0
	1	0	Clock output	fCLK
		1	Clock output	fCLK/2

9.16. Delta Sigma Modulator

The structure of Delta Sigma modulator can be selected by setting DSMSEL [1:0] bits (Table 44) and the bit length is selectable by setting OBIT [1:0] bit (Table 45). These setting bits should be changed while PMPLL bit = ”0” or RSTN bit = “0”.

Table 44. The type of Delta Sigma modulator

DSMSEL [1:0]	Type	
00	Type1	(default)
01	Type2	
10	Type3	
11	Type4	

Table 45. The bit length of output data

OBIT [1:0]	Bit length	
00	7 bits	(default)
01	6 bits	
10/11	5 bits	

Do not set DSMSEL [1:0] bits = “10” when setting OBIT [1:0] bits = “10” or “11”.
As shown in Table 46, there are prohibited gain settings depends on Delta Sigma option settings. Pop noise may occur if GC [3:0] bits are set prohibited setting.

Table 46. The relationship between Gain setting and the option of Delta Sigma modulator

(×:do not care)

DSM type DSMSEL [1:0]		Bit length OBIT [1:0]		Gain setting		
				Max	Prohibited GC [3:0] setting	
00/01	Type1/2	00	7 bits	80%	none	(default)
		01	6 bits	75%	011×	
		10/11	5 bits	62%	01××	
10	Type3	00	7 bits	56%	001×, 01××	
		01	6 bits	56%	001×, 01××	
		10/11	5 bits	Not Available		
11	Type4	00	7 bits	80%	none	
		01	6 bits	75%	011×	
		10/11	5 bits	62%	01××	

9.17. Power Up/Down Sequence

The AK4191 is powered down when the PDN pin is “L”. In power down state, all circuits stop operation and initialized, and the digital output pins becomes “L” state. The PDN pin must held “L” for more than 600 ns for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 600 ns.

When Power down is released by setting the PDN pin to “H” from “L”, Control Register block and Clock Control block start operation. In this time register access becomes available, but the digital output becomes “L” state.

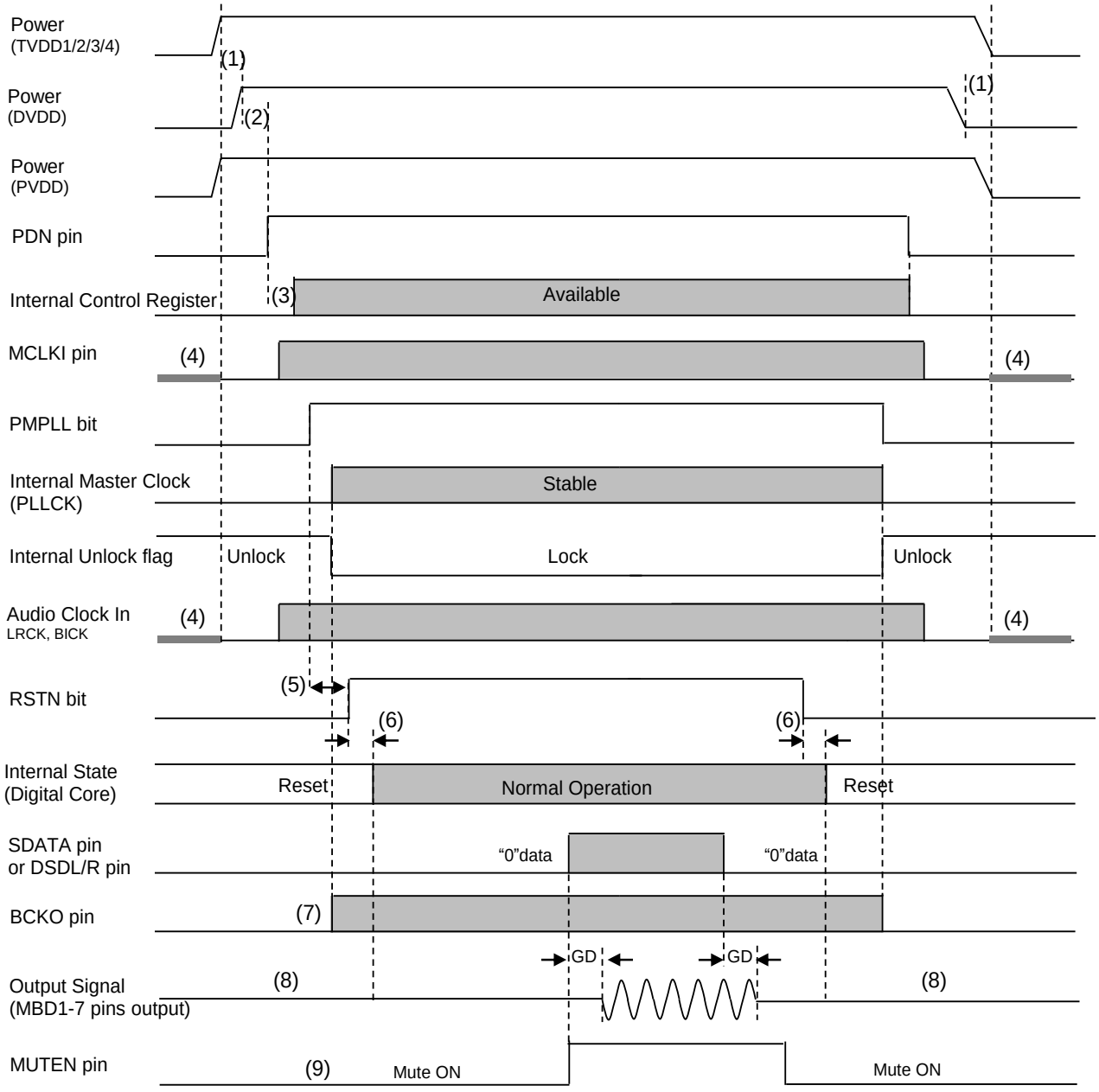
The PLL starts operation by a clock reset release (PMPLL bit = “0” → “1”) and generates the internal master clock after setting control registers. Therefore, necessary system clocks must be input before a clock reset release. The MCLK must not be stopped except during clock reset and power-down mode (PDN pin = “L”).

Clock operated circuits (All blocks except for PLL, clock control and control register) are in standby state until all three conditions shown below are satisfied.

1. Internal Master Clock is generated and stable.
2. Necessary clocks (LRCK and BICK for PCM mode, DCLK for DSD mode, BCK and WCK for EXDF mode) are supplied.
3. The RSTN bit is set to “1” from “0”.

It is recommended to set RSTN bit to “1” from “0” with an interval of 5msec (min.) for stabilization of PLL after clock reset is released. Figure 96 shows system timing example of power down/up.

9.17.1. Power Up/Down Sequence in Synchronous Mode (DSYNCE bit = "0")

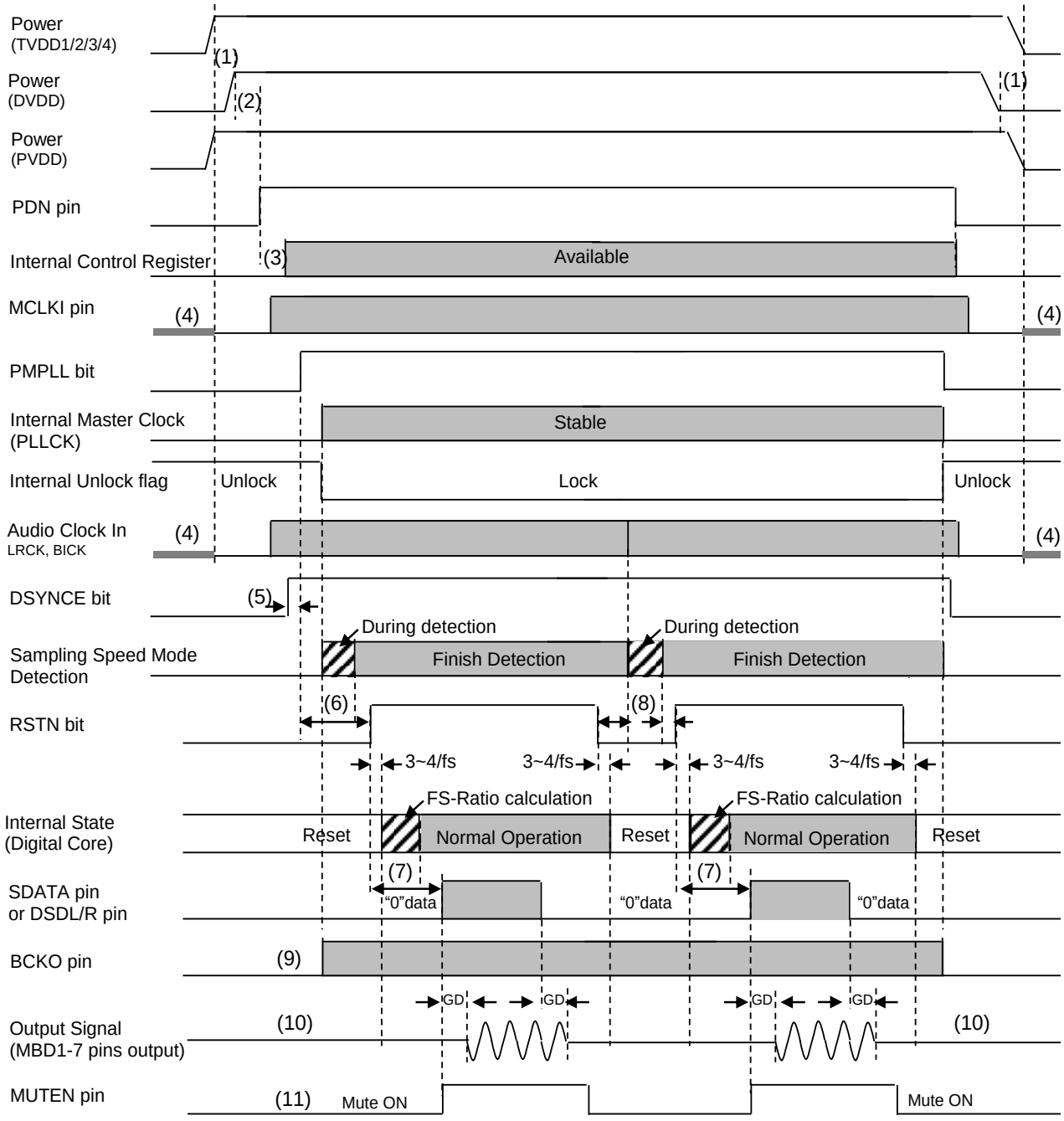


Notes:

(1) DVDD must be supplied at the same time as or after TVDD1/2/3/4. The power up sequence between PVDD, TVDD1, TVDD2, TVDD3 and TVDD4 is not critical.
(2) The PDN pin must be "L" when start supplying PVDD, DVDD and TVDD1/2/3/4. It must be held "L" for more than 600 ns after all power supplies are powered up.
(3) Register access becomes available in 1μsec (max.) after the PDN pin is set to "H".
(4) Do not input clocks (MCLK, BICK and LRCK) until after TVDD1/2/4 are turned on.
(5) It is recommended to set RSTN bit to "1" from "0" with an interval of 5msec (min.) for stabilization of PLL circuit after clock reset is released.
(6) It takes 3/fs to 4/fs until a reset instruction is valid when writing "0" to RSTN bit and it takes 3/fs to 4/fs when releasing the reset.
(7) BCKO pin output "L" when internal master clock (PLLCK) is not stable.
(8) MBD7-1 pins output "L" except normal operation state.
(9) The MUTEN pin output "L" depends on internal state. The conditions are selectable by setting MUTES [1:0] bits.

Figure 96. Power-down/up Sequence Example (Synchronous Mode)

9.17.2. Power Up/Down Sequence in Asynchronous Mode (DSYNCE bit = "1")



Notes:
(1) DVDD must be supplied at the same time as or after TVDD1/2/3/4. The power up sequence between PVDD, TVDD1, TVDD2, TVDD3 and TVDD4 is not critical.
(2) The PDN pin must be “L” when start supplying PVDD, DVDD and TVDD1/2/3/4. It must be held “L” for more than 600 nsec after all power supplies are powered up.
(3) Register access becomes available in 1μsec (max.) after the PDN pin is set to “H”.
(4) Do not input clocks (MCLK, BICK and LRCK) until after TVDD1/2/4 are turned on.
(5) DSYNCE bit should be set “1” before changing PMPLL bit = “0” to “1”.
(6) RSTN bit should be set “1” from “0” with an interval of 5msec (min.) for stabilization of PLL circuit and Sampling Speed Mode detection after clock reset is released.
(7) It is recommended to hold input data zero for 10msec until a sampling ratio calculaton for data synchronization is finished after setting RSTN bit = ”1”.
(8) LRCK frequency must be changed during AK4191 is in reset state.
(9) BCKO pin output “L” when internal master clock (PLLCK) is not stable.
(10) MBD7-1 pins output “L” except normal operation state.
(11) The MUTEN pin output “L” depends on internal state. The conditions are selectable by setting MUTES [1:0] bits.

Figure 97. Power-down/up Sequence Example (Asynchronous Mode)

9.18. Internal State

The AK4191 has six states shown in Table 47. Power Down, Standby and Reset states are controlled by PDN pin, PMPLL bit, MCLK input and RSTN bit. Unlock state depends on internal master clock (PLLCK).

Table 47. Power Down, Standby, Unlock and Reset Function (×: Do Not Care)

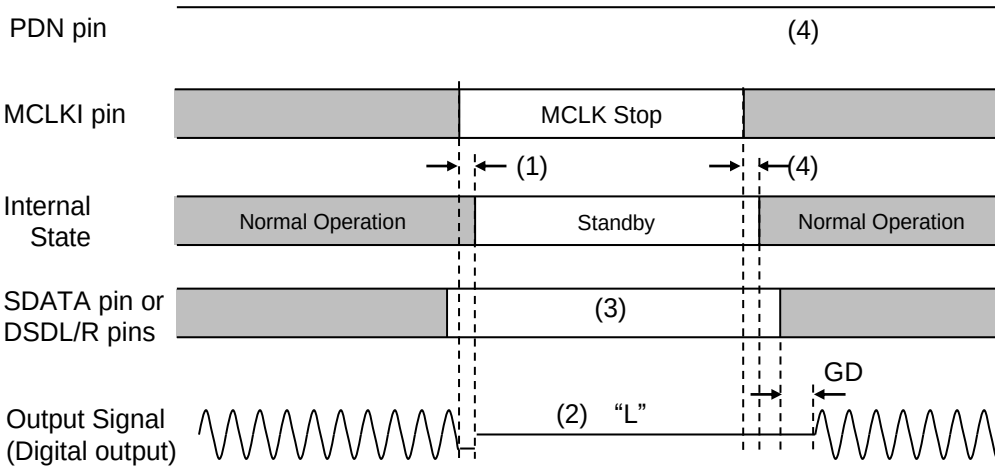
State	PDN pin	MCLK Input	PMPLL bit	Internal PLLCK	RSTN bit	Control Register	PLL	Clock Control	Digital Core	BCKO Output	MBD7-1 Output
Power Down	L	×	×	×	×	OFF	OFF	OFF	OFF	“L”	“L”
Standby	H	N	0	×	×	ON	OFF	OFF		“L”	“L”
			1	×	×		ON	OFF		“L”	“L”
		Y	0	×	×		OFF	OFF		“L”	“L”
Unlock			1	un stable	×		ON	OFF		“L”	“L”
Reset				stable	0			ON		Clock output	“L”
Normal Operation					1				ON		Signal output

When setting DSYNCE bit = “1”, Data synchronization circuit is reset if the frequency of LRCK is changed rapidly.

9.18.1. Standby Sequence by MCLK

The AK4191 has MCLK stop detection circuit. The AK4191 is automatically placed in standby state when MCLK is stopped for more than 4 μsec during normal operation (PDN pin = “H”). In this case, the digital output goes “L” (Table 47), all circuits except MCLK stop detection circuit, control register and PLL stop operation and register settings are not initialized.

When MCLK is input again, the AK4191 exits this standby state. If PMPLL bit and RSTN bit are “1” and necessary clocks (LRCK and BICK for PCM mode, DCLK for DSD mode, BCK and WCK for EXDF mode) are supplied, the AK4191 starts operation again with an interval of 5msec (min.) for stabilization of PLL circuit. The zero detection function is disabled when MCLK is stopped. Figure 98 shows standby sequence example by MCLK.

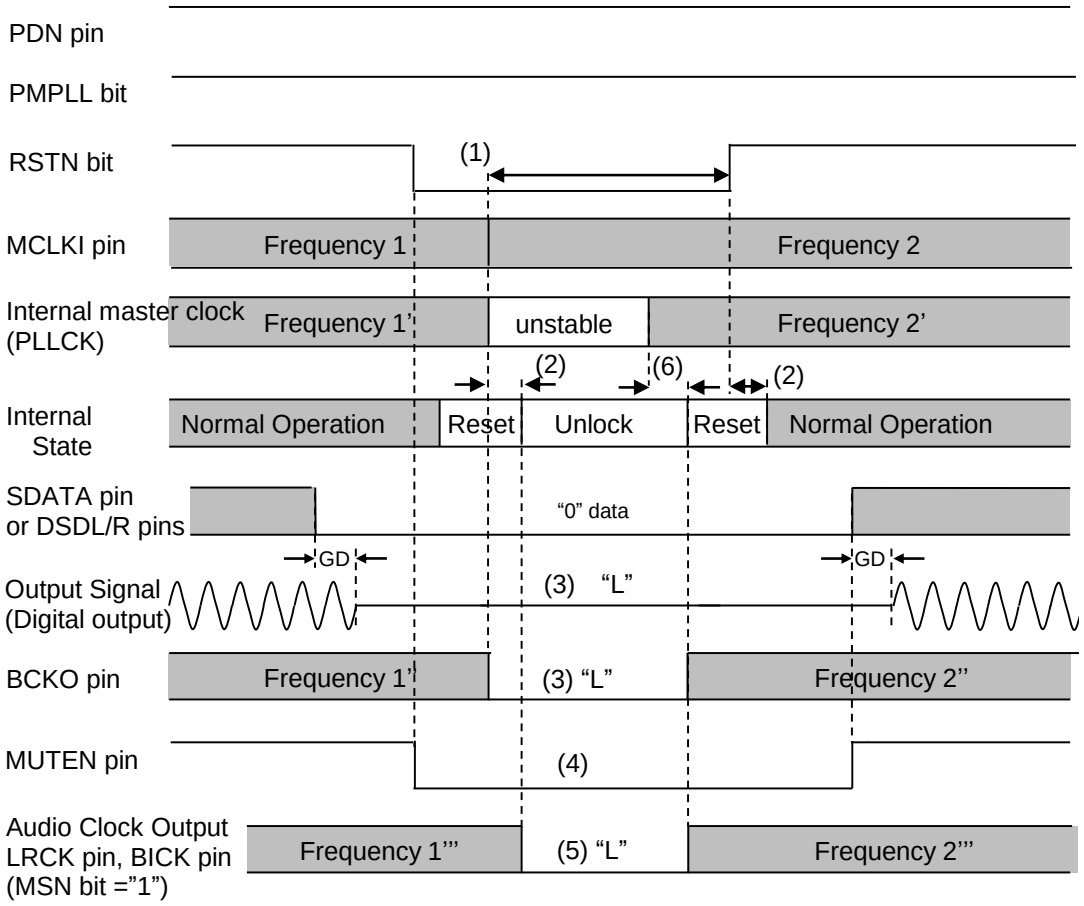


Notes:
(1) The AK4191 detects MCLK stop and becomes standby state when MCLK edge is not detected for 4 μsec (min.) during operation.
(2) The digital output goes to zero signal state (“L”) in standby state.
(3) Pop noise can be reduced by inputting “0” data when stopping and resuming MCLK supply.
(4) The AK4191 starts operation again with an interval of 5msec (min.) for stabilization of PLL circuit by resuming MCLK supply. In this case, power-up sequence by the PDN pin is not necessary.

Figure 98. Standby Sequence Example by MCLK Stop

9.18.2. Unlock Sequence (Internal master clock unstable)

AK4191 has a detection circuit for unlock state, and it is always enabled. When the frequency of internal Master Clock (PLLCK) is unstable, the AK4191 is in unlock state and clock operated circuits (All blocks except for PLL, clock control and control register) stop operation. In this case, control register access is available. The data outputs via MBD7-1 pins go to "L", but clock output via BCKO pin does not stop. Figure 99 shows unlock sequence.

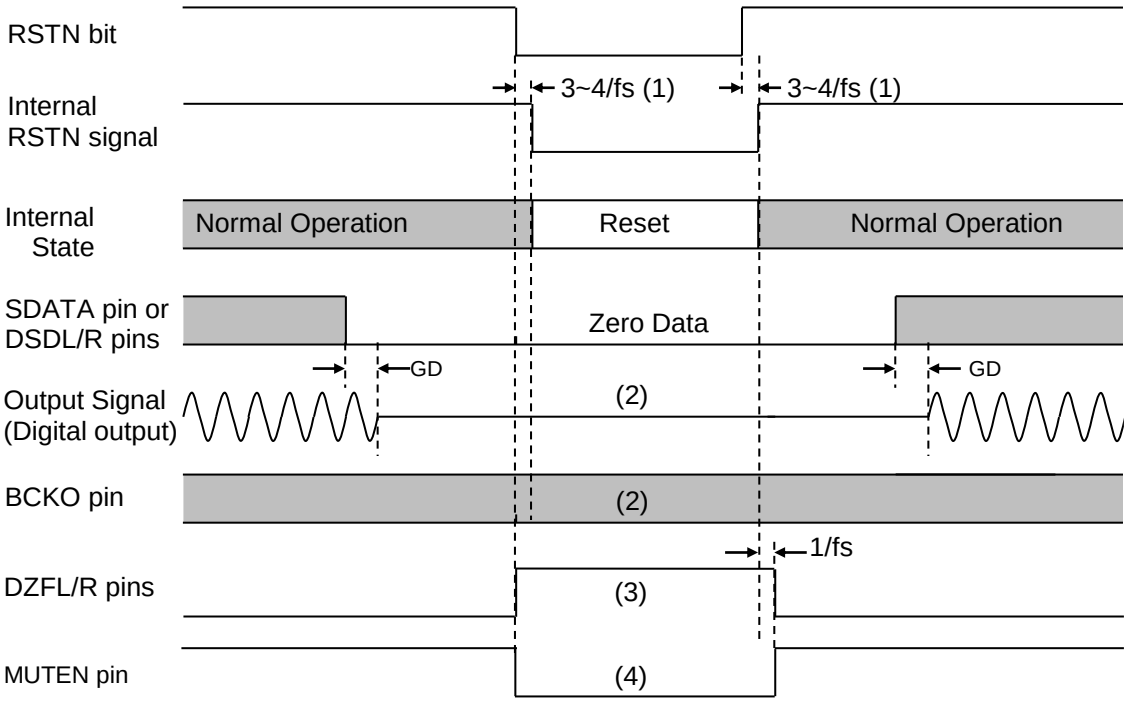


Notes:
(1) It is recommended to reset by setting RSTN bit = "0" before changing the frequency to avoid pop noise. It should be held "0" over 5 msec after changing the frequency.
(2) The AK4191 detects unlock state when the frequency of internal master clock (PLLCK) becomes unstable by changing the frequency of MCLK. It takes 5 msec.
(3) The output goes to "L" state when the AK4191 is in unlock state, but BCKO output is continued.
(4) It is possible to output reset status and unlock status flag to MUTEN pin. Refer to 9.12. Mute signal output.
(5) Audio clock outputs (LRCK pin and BICK pin) go to "L" when the AK4191 is in unlock state if MSN bit is "1".
(6) It takes 5 msec until unlock state is released after the frequency of PLLCK becomes stable.

Figure 99. Unlock state by changing the frequency of MCLK

9.18.3. Reset by RSTN bit

Digital circuits except control registers, MCLK stop detection circuit, PLL and clock control are reset by setting RSTN bit to “0”. In this case, control register settings are held, the digital output becomes zero signal output and the DZFL/DZFR pin outputs “H”. Figure 100 shows reset sequence by RSTN bit.



Notes:

(1) It takes 3/fs to 4/fs until a reset instruction is valid when changing RSTN bit to “0” and it takes 3/fs to 4/fs when releasing the reset.

(2) The output signal is zero state (“L”) when RSTN bit = “0”, but BCKO output is continued.

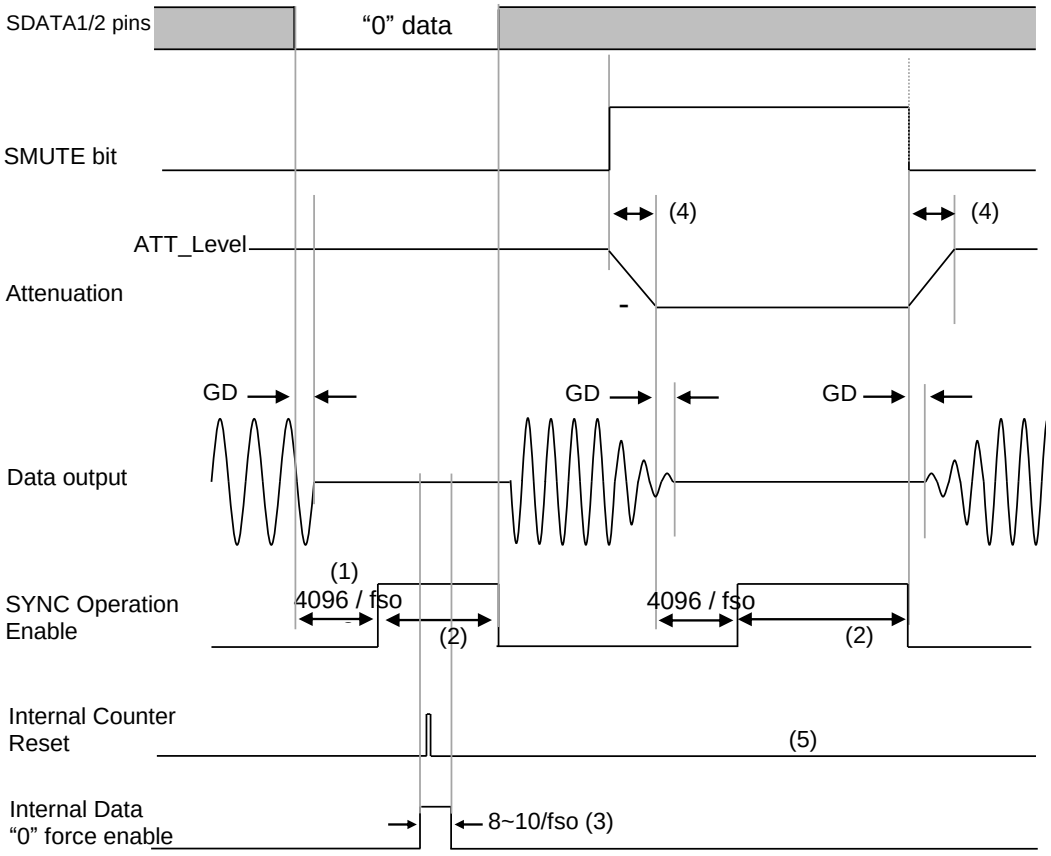
(3) This figure shows the seuqnece when DZFE bit = “1” and DDMOE bit = “0”. The DZFL/R pins go “H” on a falling edge of RSTN bit and go “L” 1/fs after a rising edge of internal RSTN bit.

(4) The MUTEN pin goes “L” on a falling edge of RSTN bit and goes “H” 1/fs after a rising edge of internal RSTN bit.

Figure 100 . Reset Timing Example

9.19. Clock Synchronize Function (PCM Mode, EXDF Mode)

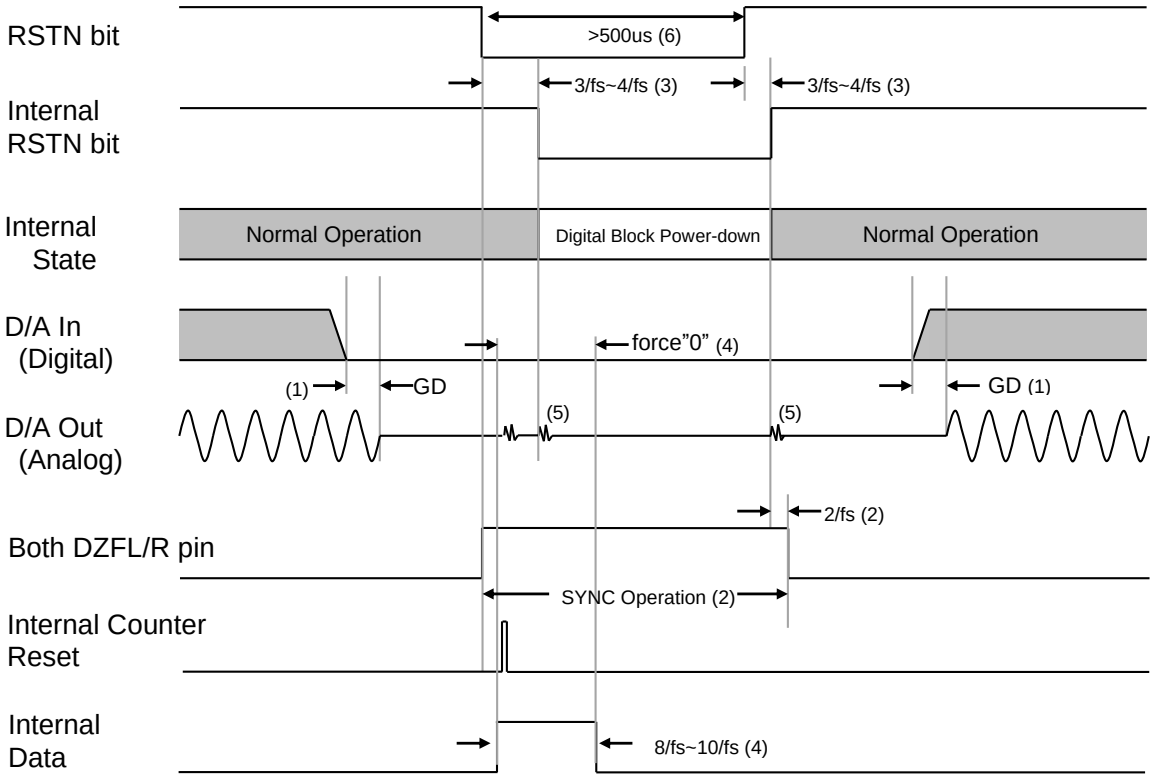
The AK4191 has a synchronize function. With this synchronize function, group delays between each device can be kept within 3 / (256 fso) when using multiple AK4191's. (fso = Base MCLK Frequency / 256)
In PCM or EXDF mode, clock synchronize function becomes valid when input data of all channels are "0" for 4096 / fso continuously, when all channels data become "0" and kept for 4096 / fso continuously by attenuation, or when RSTN bit = "0". In PCM mode, the internal clock is synchronized with a rising edge of LRCK (falling edge of LRCK when the data format is I²S compatible). In EXDF mode, the internal clock is synchronized with a rising edge of WCK. In this case, the digital output becomes zero signal. This function is disabled by setting SYNCE bit = "0" or DSYNCE = "1".
Figure 101 shows a clock synchronizing sequence when the input data is "0" for 4096 / fso continuously. Figure 102 shows a clock synchronizing sequence by RSTN bit.



Notes:
(1) When all channels data are "0" for 4096 / fso continuously, the synchronize function is enabled.
(2) To ensure the synchronization, zero data input should be kept for 500 µsec at least after the synchronize function is enabled.
(3) Input data of ΔΣ Modulator is fixed to "0" forcibly for 8/fso to 10/fso when internal counter is reset.
(4) Refer to "9.6. Digital Attenuator" for ATT transition time.
(5) When the internal clock and external input clock are in synchronization, the internal counter will not be reset even if the synchronize function is valid.

Figure 101. Synchronization Sequence by Continuous "0" Data Input for 4096 / fso

If RSTN bit is set to “0”, digital circuit is reset in 3/fs to 4/fs and the synchronization function becomes valid.



Notes:

(1) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to RSTN bit.
(2) The synchronization function becomes valid on a falling edge of RSTN bit. It takes about 2/fs to become invalid after the internal RSTN is changed when changing RSTN bit to “1”.
(3) It takes 3/fs to 4/fs until the internal RSTN is changed when changing RSTN bit to “0” and it takes 3/fs to 4/fs when changing RSTN bit to “1”. The synchronization function becomes valid immediately when writing “0” to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.
(4) Input data of ΔΣ Modulator is fixed to “0” forcibly for 8/fs to 10/fs when the internal counter is reset.
(5) Pop noise occurs on rising and falling edges of the internal RSTN signal and when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this pop noise affects the system performance.
(6) To ensure the synchronization, reset state should be kept for 500 μsec at least after the synchronize function is enabled.

Figure 102. Synchronization Sequence by RSTN bit (Register Control Mode)

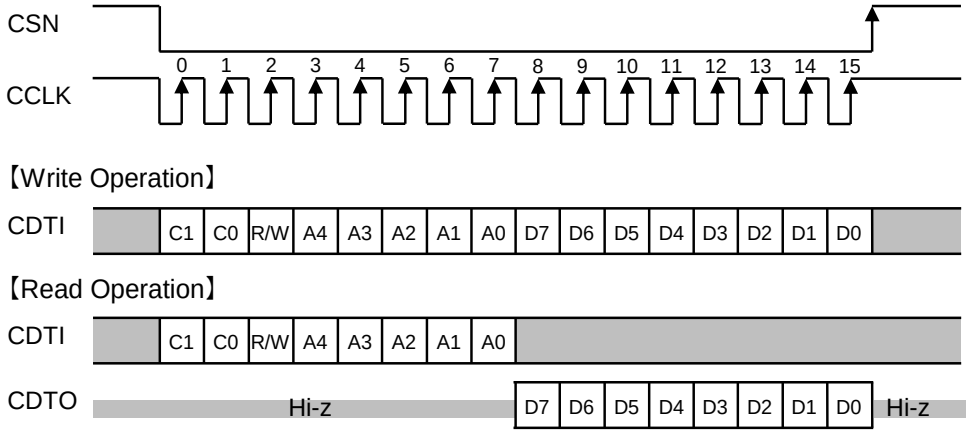
9.20. Control Interface

The AK4191 has register control interface. This interface is enabled when PDN pin is “H” and PROG pin is “L”. Control interface mode can be switched by I2C pin. I2C pin should be set while PDN pin is “L”. Setting PDN pin to “L” resets the registers to their default values. The digital block except control registers and clock divider is reset by setting RSTN bit to “0”. In this case, the register values are not initialized. When PROG pin is “H”, it is not possible to access the registers, but the register values are kept.

PROG pin	I2C pin	Interface	Access Mode
L	L	4-wire µP	Register Control
	H	I2C-Bus	Register Control
H	L	4-wire µP	Programmable Filter Coefficients Memory
	H	Not Available	

9.20.1. 4-wire Serial Register Control Mode (PROG pin = "L", I2C pin = “L”)

Internal registers may be written to through 4-wire µP interface pins: CSN, CCLK, CDTI and CDTO. The data on this interface consists of Chip address (2-bit, C1/0), Read/Write (1-bit), Register address (MSB first, 5-bit) and Control data (MSB first, 8-bit). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN “↑”. For read operations, the CDTO output goes high impedance after a low to high transition of CSN. The clock speed of CCLK is 5 MHz (max).



C1-0: Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0 pin)
R/W: READ/WRITE (“1” : Write, “0” : Read)
A4-0: Register Address
D7-0: Control Data

Figure 103. Control I/F Timing

* When the PDN pin = “L”, writing into control registers is prohibited.
* The control data cannot be written when the CCLK rising edge is 15 times or less, or 17 times or more during CSN is “L”.

9.20.2. I²C Bus Register Control Mode (PROG pin = "L", I2C pin = "H")

The AK4191 supports the fast-mode I²C-bus (max:400 kHz).

9.20.2.1. WRITE Operation

Figure 104 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 110). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 105). If the slave address matches that of the AK4191, the AK4191 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 111). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4191 and the format is MSB first. The most significant three bits are fixed as "000" (Figure 106). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 107). The AK4191 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 110).

The AK4191 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4191 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "16H" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 112) except for the START and STOP conditions.

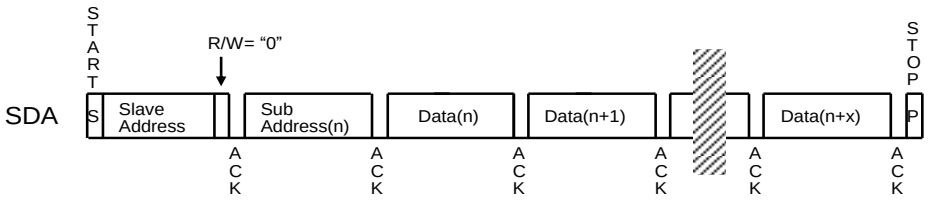


Figure 104. Data Transfer Sequence in I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1 and CAD0 are set by pin)

Figure 105. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 106. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 107. Byte Structure after The Second Byte

9.20.2.2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4191. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4191 supports two basic read operations: Current Address Read and Random Address Read.

9.20.2.2.1. Current Address Read

The AK4191 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4191 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4191 ceases the transmission.

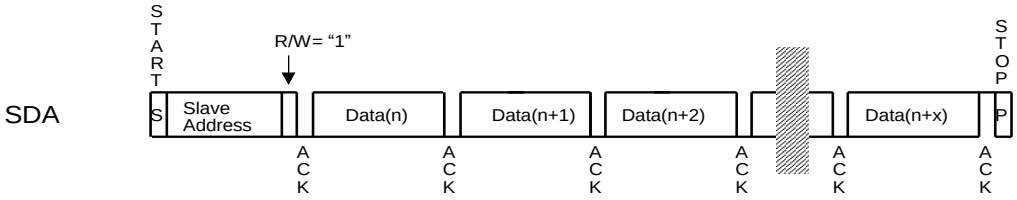


Figure 108. Current Address Read

9.20.2.2.2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4191 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4191 ceases the transmission.

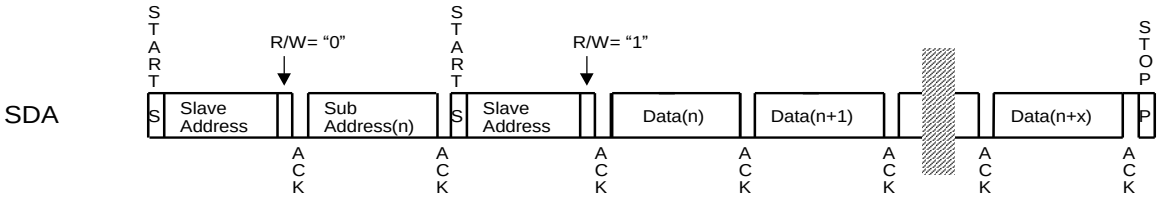


Figure 109. Random Address Read

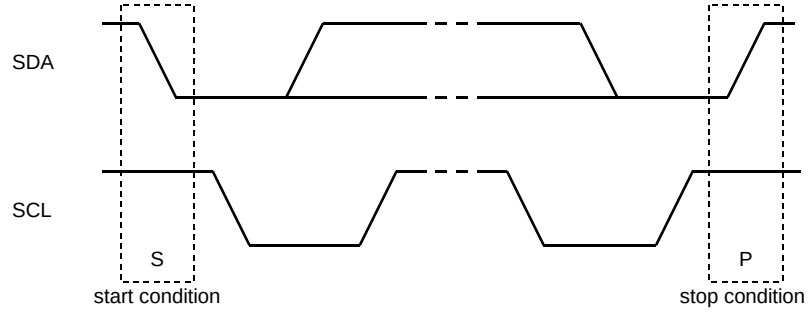


Figure 110. Start Condition and Stop Condition

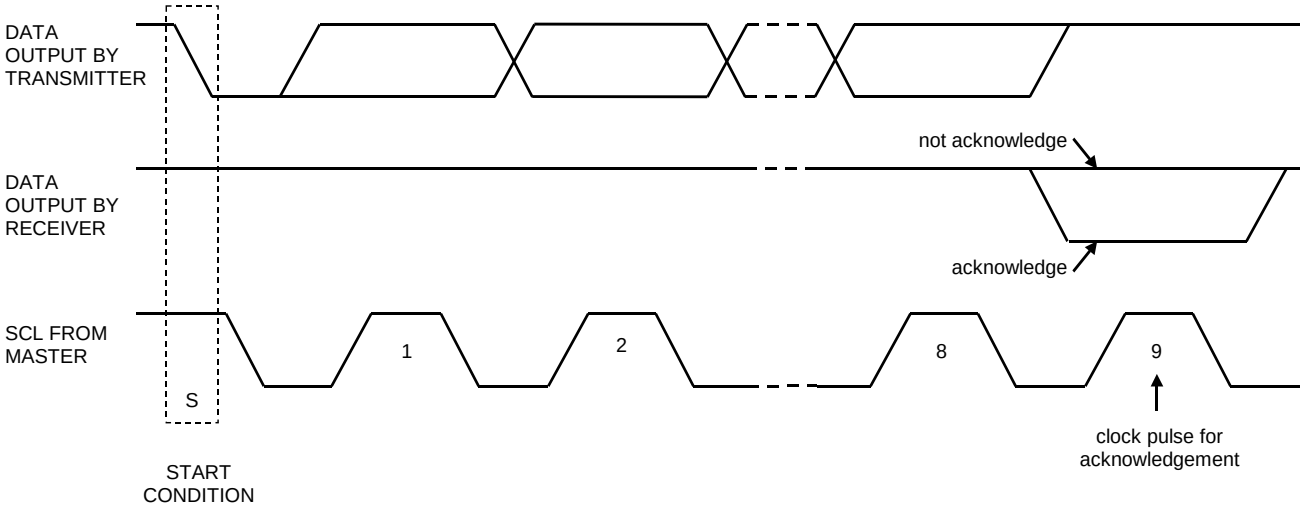


Figure 111. Acknowledge (I^2C Bus)

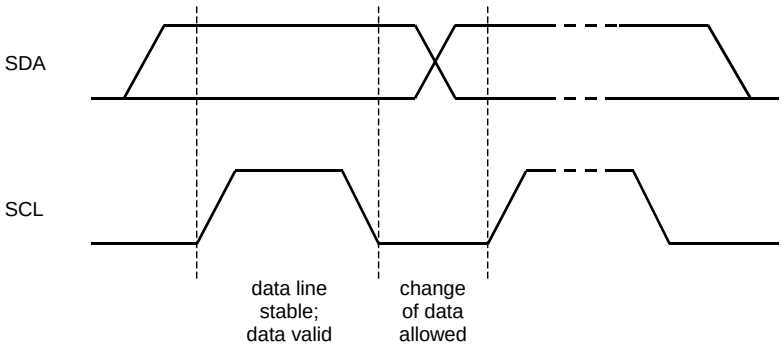


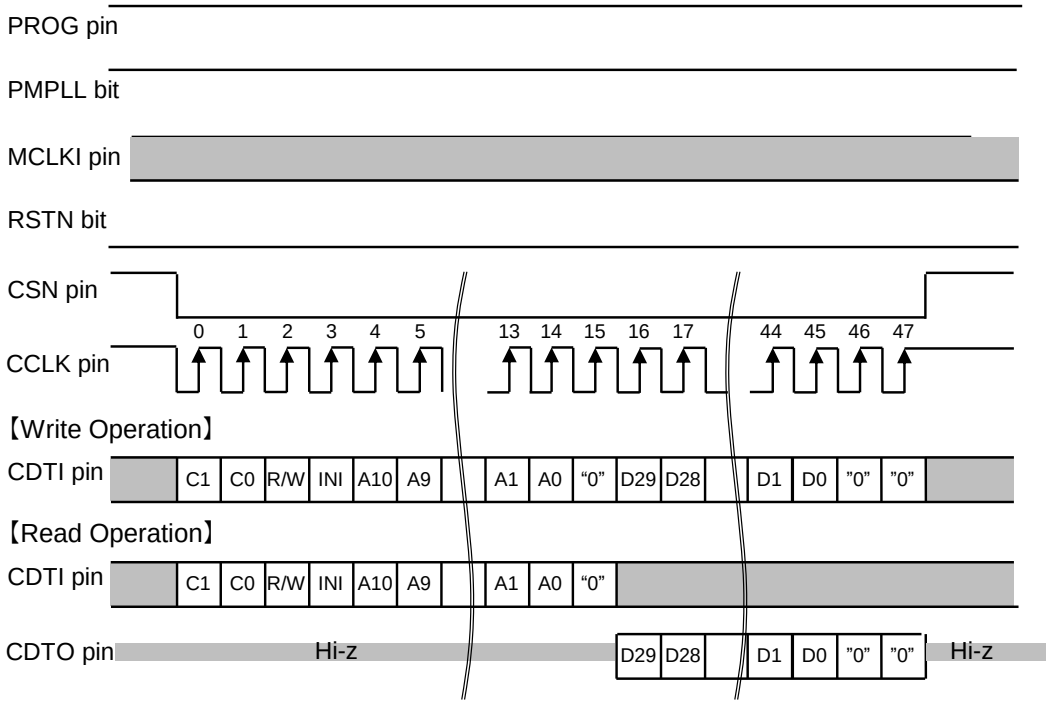
Figure 112. Bit Transfer (I^2C Bus)

9.20.3. Programmable Filter Coefficients Access Mode (PROG pin = “H”)

The AK4191 has the coefficients memory. It should be written before using Programmable Filter. It is enabled to access the coefficients memory by setting PROG pin “H”. In this mode, it is disabled to access Register Control Interface (9.20 Control Interface), but the values of control registers are kept.

MCLK must be supplied, PMPLL bit must be “1”, internal master clock (PLLCK) must be stable and RSTN bit should be “0” when access the coefficients memory. They may be written to through CSN pin, CCLK pin and CDTI pin when PROG pin is "H". The data on this interface consists of Chip address (2 bits, C1/0), Read/Write (1 bit), Initialize setting bit (1bit), Coefficients word address (MSB first, 11 bits), 1bit ”0”, Coefficients data (MSB first, 30 bits) and 2bits “00”. The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The clock speed of CCLK is 5 MHz (max).

The size of memory is 30 bits × 1280 words in 1×/2×/4× sampling speed mode and 30 bits × 316 words in 8×/16× sampling speed mode. They are not initialized by setting PDN pin = “L” or RSTN bit = “0”, but may be initialized zero by setting INI bit = ”1” over 80μs. R/W bit should be “0” when changing the value of INI bit.

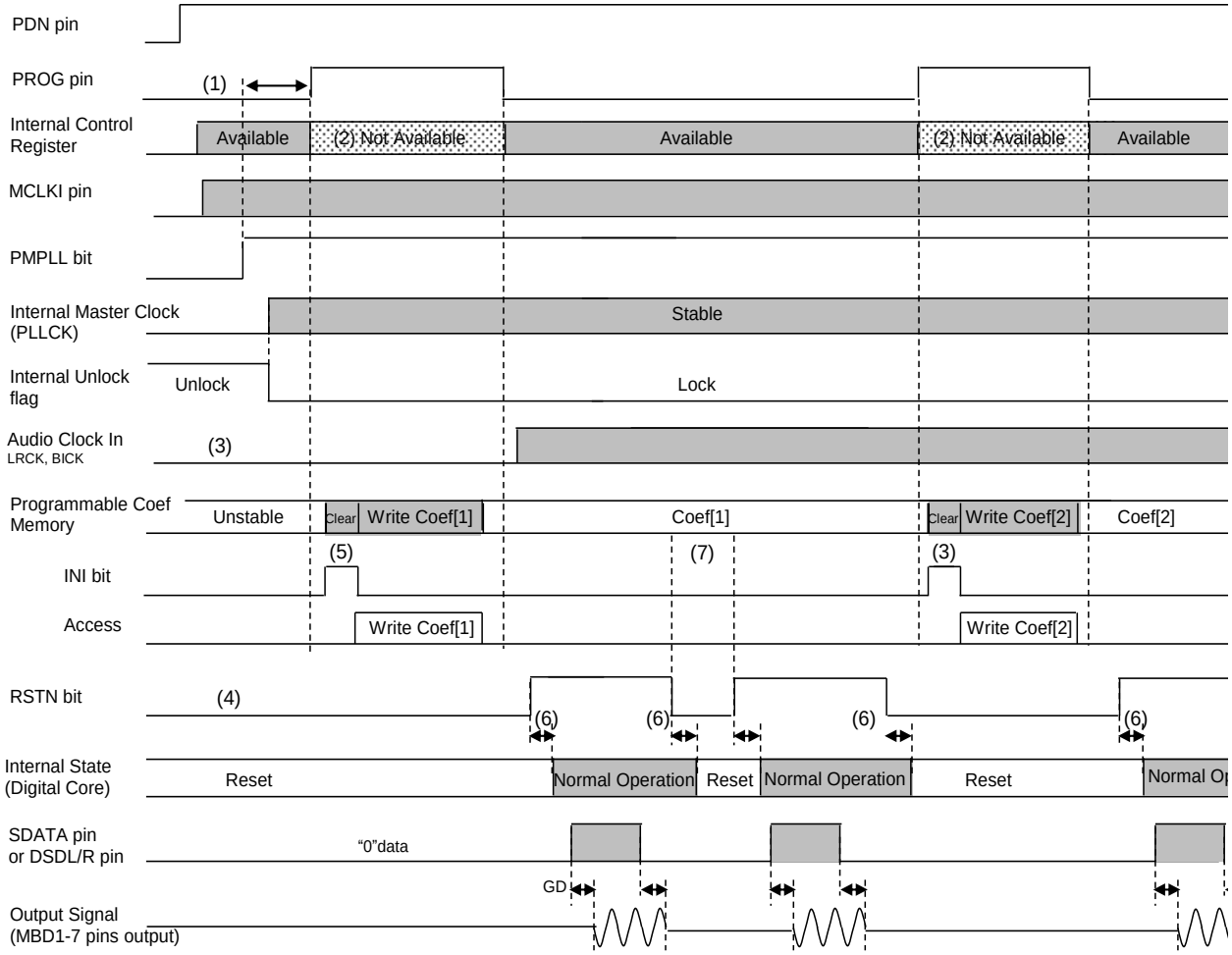


C1-0:	Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0 pin)
R/W:	READ/WRITE (“1”: Write, “0”: Read)
INI:	Coefficients memory Initialize sequence (“1”: ON, “0”: OFF)
A10-0:	Coefficients Address
D29-0:	Coefficients Data

Notes :

* When the PDN pin = “L”, writing into control registers is prohibited.
* RSTN bit should be “0”, MCLK should be supplied and PMPLL bit should be “1” when access the coefficients memory.
* The writing of data is stored at the timing between 46th CCLK “↑” and CSN “↑” by using internal PLLCK.

Figure 113. Programmable Filter Coefficients I/F timing



Notes:
(1) PROG pin should be held "L" over 5 msec after setting PMPLL bit "1".
(2) Control Register is not acceptable during PROG pin is "H", but the values of control registers are kept.
(3) Audio clock inputs (LRCK pin, BICK pin, WCK pin, BCK pin, DCLK pin) are not necessary to access Programmable Filter Coefficients Memory.
(4) RSTN bit should be "0" during PROG pin is "H".
(5) Programmable Filter Coefficients Memory should be initialized by setting INI bit "1".
(6) It takes 3/fs to 4/fs until a reset instruction is valid when changing RSTN bit to "0" and it takes 3/fs to 4/fs when releasing the reset.
(7) Programmable Filter Coefficients are kept when setting RSTN bit "0".

Figure 114. Timing Example of using Programmable Filter

9.20.4. Programmable Filter Coefficients

The AK4191 has a multi-rate FIR filter and the 1st stage coefficients of the multi-rate filter are programmable. The programmable filter must satisfy following conditions shown in Table 48.
The operating procedure to write coefficients is shown in 9.20.3. Programmable Filter Coefficients Access Mode (PROG pin = "H")

Table 48. Programmable Filter Specifications

		1×/2×/4× Speed Mode (PCM mode)	8×/16× Speed Mode (PCM and EXDF mode)
Filter specifications			
	Oversampling Rate	16×	4×
	Interpolation method	zero data interpolation	zero data interpolation
	The maximum filter DC gain	0 dB	0 dB
	The maximum filter passband ripple	+0.1 dB	+0.1 dB
Filter Coefficients specifications			
	Data type	2's compliment	2's compliment
	Bit Length	30 bits	30 bits
	The Maximum filter taps	1280	316
	The sum of all coefficients to obtain 0dB filter DC gain	$16 * 2^{29} - 1$	$4 * 2^{29} - 1$
	Absolute value summation	$\sum_{n=0}^{79} \lvert h(16n+k) \rvert < 4 * 2^{29}$ $(k = 0,1,2 \cdot \cdot 15)$ (Note 25)	$\sum_{n=0}^{78} \lvert h(4n+k) \rvert < 4 * 2^{29}$ $(k = 0,1,2,3)$ (Note 26)

Note 25. Expression $\sum_{n=0}^{79} \lvert h(16n+k) \rvert \ (k = 0,1,2 \cdot \cdot 15)$ means following.

$$k = 0: \quad \sum_{n=0}^{79} \lvert h(16n+0) \rvert = \lvert h(0) \rvert + \lvert h(16) \rvert + \lvert h(32) \rvert \cdot \cdot \cdot + \lvert h(1264) \rvert$$

$$k = 1: \quad \sum_{n=0}^{79} \lvert h(16n+1) \rvert = \lvert h(1) \rvert + \lvert h(17) \rvert + \lvert h(33) \rvert \cdot \cdot \cdot + \lvert h(1265) \rvert$$

$$\vdots$$

$$k = 15: \quad \sum_{n=0}^{79} \lvert h(16n+15) \rvert = \lvert h(15) \rvert + \lvert h(31) \rvert + \lvert h(47) \rvert \cdot \cdot \cdot + \lvert h(1279) \rvert$$

Note 26. Expression $\sum_{n=0}^{78} \lvert h(4n+k) \rvert \ (k = 0,1,2,3)$ means following.

$$k = 0: \quad \sum_{n=0}^{78} \lvert h(4n+0) \rvert = \lvert h(0) \rvert + \lvert h(4) \rvert + \lvert h(8) \rvert \cdot \cdot \cdot + \lvert h(312) \rvert$$

$$k = 1: \quad \sum_{n=0}^{78} \lvert h(4n+1) \rvert = \lvert h(1) \rvert + \lvert h(5) \rvert + \lvert h(9) \rvert \cdot \cdot \cdot + \lvert h(313) \rvert$$

$$k = 2: \quad \sum_{n=0}^{78} \lvert h(4n+2) \rvert = \lvert h(2) \rvert + \lvert h(6) \rvert + \lvert h(10) \rvert \cdot \cdot \cdot + \lvert h(314) \rvert$$

$$k = 3: \quad \sum_{n=0}^{78} \lvert h(4n+3) \rvert = \lvert h(3) \rvert + \lvert h(7) \rvert + \lvert h(11) \rvert \cdot \cdot \cdot + \lvert h(315) \rvert$$

9.21. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	Control 1	DUAL	EXDF	MUTES[1]	MUTES[0]	DIF[2]	DIF[1]	DIF[0]	RSTN	0CH
01H	Control 2	0	0	SSLOW	SD	SLOW	DEM[1]	DEM[0]	SMUTE	12H
02H	Control 3	DP	ADP	0	DCKB	DDMOE	DZFE	DZFM	DZFB	00H
03H	Lch ATT	ATTL[7]	ATTL[6]	ATTL[5]	ATTL[4]	ATTL[3]	ATTL[2]	ATTL[1]	ATTL[0]	FFH
04H	Rch ATT	ATTR[7]	ATTR[6]	ATTR[5]	ATTR[4]	ATTR[3]	ATTR[2]	ATTR[1]	ATTR[0]	FFH
05H	Control 4	INVL	INVR	SELLR	MONO	DFS[2]	DFS[1]	DFS[0]	MSN	00H
06H	DSD1	DDM	DML	DMR	DDMT	DSDD	DSDSEL [2]	DSDSEL [1]	DSDSEL [0]	00H
07H	Control 5	ATS[1]	ATS[0]	0	GC[3]	GC[2]	GC[1]	GC[0]	SYNCE	01H
08H	Control 6	BCKS[1]	BCKS[0]	MCKOE	MCKDV	MCKS[1]	MCKS[0]	FS32K	PMPLL	00H
09H	DSD2	0	0	0	0	0	0	DSDF	DSDPATH	00H
0AH	Control 7	TDM[1]	TDM[0]	SDS[2]	SDS[1]	SDS[0]	0	OSTME	ISTME	00H
0BH	Control 8	0	0	0	0	0	0	0	DSYNCE	00H
0CH	DSMI/O	DSMIFS	MBDZ	DSMSEL [1]	DSMSEL [0]	0	OBIT[1]	OBIT[0]	OSR	00H
0DH	DSMI	ATSMX[1]	ATSMX[0]	GAIN2L	GAIN2R	IBIT	SUBL	SUBR	PMDSMI	00H
0EH	FB ATTL	ATTMXL [7]	ATTMXL [6]	ATTMXL [5]	ATTMXL [4]	ATTMXL [3]	ATTMXL [2]	ATTMXL [1]	ATTMXL [0]	00H
0FH	FB ATTR	ATTMXR [7]	ATTMXR [6]	ATTMXR [5]	ATTMXR [4]	ATTMXR [3]	ATTMXR [2]	ATTMXR [1]	ATTMXR [0]	00H
10H	Reserved	DSEL[7]	DSEL[6]	DSEL[5]	DSEL[4]	DSEL[3]	DSEL[2]	DSEL[1]	DSEL[0]	00H
11H	Reserved	0	0	0	0	0	0	0	0	00H
12H	Reserved	0	0	0	0	0	0	0	0	00H
13H	Reserved	0	0	0	0	0	0	0	0	00H
14H	Reserved	0	0	0	0	0	0	0	0	00H
15H	Control 9	ADPE	ADPT[1]	ADPT[0]	0	0	ADFS[2]	ADFS[1]	ADFS[0]	00H
16H	Control 10	0	0	0	0	ADCKS	ADSDS[2]	ADSDS[1]	ADSDS[0]	00H

Notes:

(1) If the address exceeds “16H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H” by automatic increment function in I^2C-Bus mode.
(2) Bits indicated as 0 in each address must contain a “0” value. Malfunctions may occur if writing “1” value to these bits.
(3) Writing after 17H is forbidden. Malfunctions may also occur by this action.
(4) When the PDN pin goes to “L”, the registers are initialized to their default values.
(5) When RSTN bit is set to “0”, the digital block except control registers and clock divider is reset, and the registers are not initialized to their default values.

9.22. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	DUAL	EXDF	MUTES [1]	MUTES [0]	DIF [2]	DIF [1]	DIF [0]	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF [2:0]: Audio Data Interface modes (Table 20Table 20)
Initial value is “110” (Mode 6: 32bit MSB justified)

MUTES [1:0]: MUTEN pin Output condition setting (Table 39)

EXDF: External Digital Filter I/F Mode
0: Disable: Internal Digital Filter mode (default)
1: Enable: External Digital Filter mode

DUAL: Audio Data Dual Input Mode
0: Single Input Mode (default)
1: Dual Input Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SSLOW	SD	SLOW	DEM [1]	DEM [0]	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM1[1:0]: DAC De-emphasis Filter Control (Table 25)
Initial value is “01” (OFF).

SLOW: Slow Roll-off Filter Enable (Table 23)
0: Sharp Roll-off filter (default)
1: Slow Roll-off filter

SD: Short Delay Filter Enable (Table 23)
0: Traditional filter
1: Short Delay filter (default)

SSLOW: Super Slow Roll-off (Digital Filter bypass mode) or Low Dispersion Filter Enable (Table 23)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	0	DCKB	DDMOE	DZFE	DZFM	DZFB
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DZFB: Inverting Enable of DZF (Table 30)
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

DZFM: Output select for DZFL/R pins (Table 29)

DZFE: Output select for DZFL/R pins (Table 29)

DDMOE: Zero Detection/DSD Signal Full-scale Detection Flag Selection (Table 29)

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

ADP: Read Back register for internal operation mode. This bit is valid when ADPE bit = “1”.
It is invalid when ADPE bit = “0” and readouts “0” when read.
0: PCM mode/EXDF mode
1: DSD Mode

DP: DSD/PCM Mode Select
0: PCM mode (default)
1: DSD mode
When DP bit is changed, the AK4191 should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATTL [7]	ATTL [6]	ATTL [5]	ATTL [4]	ATTL [3]	ATTL [2]	ATTL [1]	ATTL [0]
04H	Rch ATT	ATTR [7]	ATTR [6]	ATTR [5]	ATTR [4]	ATTR [3]	ATTR [2]	ATTR [1]	ATTR [0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL [7:0]: DAC L channel Attenuation Level setting (Table 26)
ATTR [7:0]: DAC R channel Attenuation Level setting (Table 26)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL	INVR	SELLR	MONO	DFS [2]	DFS [1]	DFS [0]	MSN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSN: Master / Slave mode setting
0: Slave mode (default)
1: Master mode

DFS [2:0]: Sampling Speed Control (Table 12, Table 13, Table 17, Table 18)
These settings are valid when MSN bit is “1”.
Initial value is “000” (1× speed mode).
A pop noise occurs when changing DFS [2:0] bits setting.

MONO: DAC Mono/Stereo mode select (Table 34)
0: Stereo mode (default)
1: Mono mode

SELLR: DAC data selection of L channel and R channel (Table 34)

INVR: Signal Output Phase Inverting (Table 34)
0: Disable (default)
1: Enable

INVL: Signal Output Phase Inverting (Table 34)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML	DMR	DDMT	DSDD	DSDSEL [2]	DSDSEL [1]	DSDSEL [0]
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL [2:0]: DSD sampling speed control (Table 14)

DSDD: DSD Playback Path Control
0: Normal Path (default)
1: Volume Bypass

DDMT: DSD Signal Full-scale Detection Time Setting (Table 32)

DMR/L: This register outputs detection flag when a full-scale is detected at the DSDR pin /DSDL pin.

DDM: DSD data mute
The AK4191 has an internal mute function that mutes the output when DSD input data becomes all “1” or all “0” for 2048 samples (1/fs) continuously. DDM bit controls this function.
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	ATS [1]	ATS [0]	0	GC [3]	GC [2]	GC [1]	GC [0]	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: SYNC Mode Enable
0: SYNC mode Disable
1: SYNC mode Enable (default)

GC [3:0]: Gain Control (Table 28)

ATS [1:0]: Transition Time Between Set Values of ATTL/R [7:0] bits (Table 27)
Initial value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Control 6	BCKS [1]	BCKS [0]	MCKOE	MCKDV	MCKS [1]	MCKS [0]	FS32K	PMPLL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: Power management of PLL
0: PLL off (default)
1: PLL on

FS32K: Sampling Frequency setting (Table 7, Table 8)
0: Base Sampling Frequency is 42kHz to 54kHz (default)
1: Base Sampling Frequency is 30kHz to 34kHz

MCKS [1:0]: System Clock Setting (Table 7)
Initial value is “00” (12.288 or 11.2896 MHz).

MCKDV: MCLKO frequency setting (Table 43)
Initial value is “0” (MCLKO frequency is same as MCLK).

MCKOE: MCLKO Output Enable
0: Disable (default)
1: Enable

BCKS[1:0]: BICK/BCK Frequency Setting (Table 12, Table 13, Table 17, Table 18)
Initial value is “00” (128fs).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDPATH
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDPATH: DSD data input pin select (Table 3)

DSDF: Cut-off frequency of DSD Filter control (Table 24)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 7	TDM [1]	TDM [0]	SDS [2]	SDS [1]	SDS [0]	0	OSTME	ISTME
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ISTME: Delta Sigma Modulator Data Input (DSMI) format setting
0: MONO mode (default)
1: Stereo mode

OSTME: Delta Sigma Modulator Data Output (MBD) format setting
0: MONO mode (default)
1: Stereo mode

SDS [2:0]: Output Data Slot Selection of Each Channel (Table 21)

TDM [1:0]: TDM Mode Select
00: Normal (default)
01: TDM128
10: TDM256
11: TDM512

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 8	0	0	0	0	0	0	0	DSYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSYNCE: Data Synchronization Function Setting (Table 4)
0: Synchronization disable (default)
1: Synchronization enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	DSMI/O	DSMIFS	MBDZ	DSMSEL [1]	DSMSEL [0]	0	OBIT [1]	OBIT [0]	OSR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

OSR: BCKO Frequency Setting (Table 9)
Initial value is “0” (BCKO frequency is 12.288 or 11.2896 MHz).

OBIT [1:0]: Delta Sigma Modulator Data Output (MBD7-1) Bit Number
00: 7 bits (default)
01: 6 bits
10/11: 5 bits

DSMSEL [1:0]: Delta Sigma Modulator Data Output (MBD7-1) Selection Type (Table 44)
00: Type 1 (default)
01: Type 2
10: Type 3
11: Type 4

MBDZ: Delta Sigma Modulator Data Output (MBD7-1) zero function setting
0: off (default)
1: force MBD7-1 zero when MUTEN pin outputs “L”.

DSMIFS: Delta Sigma Modulator Data Input Frequency (BCKI) Setting
0: 256 fs (BCKI frequency is 12.288 or 11.2896 MHz) (default)
1: 128 fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	DSMI	ATSMX [1]	ATSMX [0]	GAIN2L	GAIN2R	IBIT	SUBL	SUBR	PMDSMI
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMDSMI: Delta Sigma Modulator Data Mix Function Power management (Table 40)
Initial value is "0" (Data Mix Function off)

SUBL/R: Delta Sigma Modulator Data Mix Function Polarity (Table 40)
Initial value is "0" (Add Data)

IBIT: Delta Sigma Modulator Data Input (DSMI1-7) Bit Number
0: 7 bits (default)
1: 6 bits

GAIN2L/R: Gain Control of Delta Sigma Modulator Data Mix Function (Table 41)
Initial value is "0" (0dB)

ATSMX [1:0]: Transition Time Between Set Values of ATTMXL/R [7:0] bits (Table 42)
Initial value is "00"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	FB ATTL	ATTMXL [7]	ATTMXL [6]	ATTMXL [5]	ATTMXL [4]	ATTMXL [3]	ATTMXL [2]	ATTMXL [1]	ATTMXL [0]
0FH	FB ATTR	ATTMXR [7]	ATTMXR [6]	ATTMXR [5]	ATTMXR [4]	ATTMXR [3]	ATTMXR [2]	ATTMXR [1]	ATTMXR [0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTMXL [7:0]: L channel Mix Data Attenuation Level setting (Table 41)
ATTMXR [7:0]: R channel Mix Data Attenuation Level setting (Table 41)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Reserved	DSEL [7]	DSEL [6]	DSEL [5]	DSEL [4]	DSEL [3]	DSEL [2]	DSEL [1]	DSEL [0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

10H: This address is set to 21H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

11H: Reserved
12H: Reserved
13H: Reserved
14H: Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Control 9	ADPE	ADPT [1]	ADPT [0]	0	0	ADFS [2]	ADFS [1]	ADFS [0]
R/W		R/W	R/W	R/W	R/W	R/W	R	R	R
Default		0	0	0	0	0	0	0	0

ADFS [2:0]: fs Auto Detect Mode Detection Result (Table 11)

ADPT[1:0]: Time until PCM/DSD mode detection when input data becomes zero (PCM/EXDF⇔DSD modes) (Table 36)

ADPE: Automatic Mode Switching Function Enable Bit for PCM/EXDF and DSD Modes
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Control 10	0	0	0	0	ADCKS	ADSDS [2]	ADSDS [1]	ADSDS [0]
R/W		R/W	R/W	R/W	R/W	R/W	R	R	R
Default		0	0	0	0	0	0	0	0

ADSDS[2:0]: fs Auto Detect Mode Detection Result for DSD Modes (Table 11, Table 15)

ADCKS: fs Auto Detect Mode Detect Function Enable Bit for DSD Modes
0: Disable (default)
1: Enable

10. Recommended External Circuits

10.1. External Connection Example

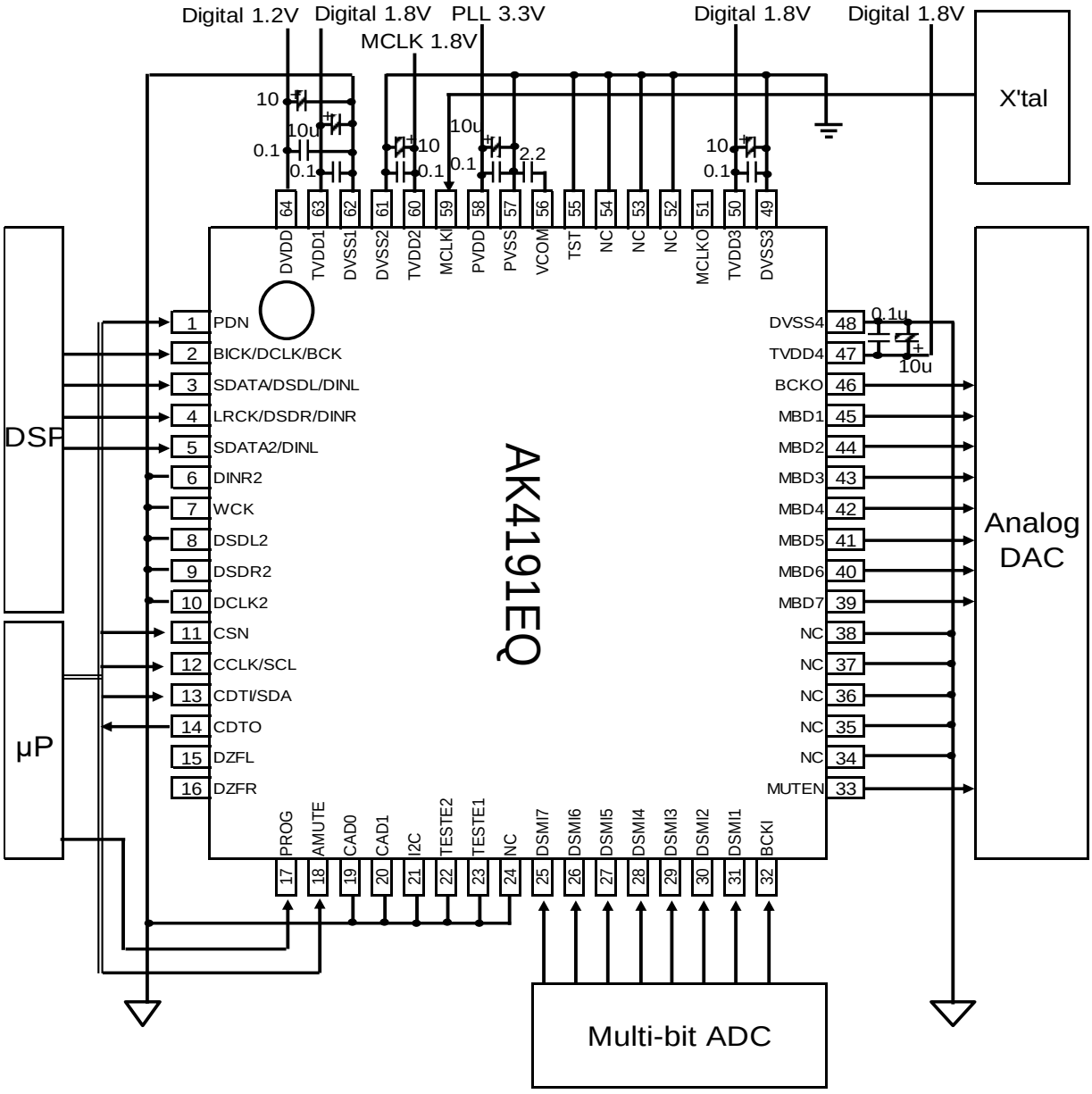


Figure 115. Typical Connection Diagram
(PVDD = 3.3 V, TVDD1 = 1.8 V, TVDD2 = 1.8 V, TVDD3 = 1.8 V, TVDD4 = 1.8 V, DVDD = 1.2 V)

Notes:
(1) Chip Address = “00”.
(2) Power lines of PVDD, TVDD1/2/3/4 and DVDD should be distributed separately, from the point with low impedance of regulators or other parts.
(3) PVSS and DVSS1/2/3/4 must be connected to the same ground plane. (Ground should have low impedance as a solid pattern.
(4) It is recommended to output MBD7-1 and BCK via a 51Ω damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of these data.
(5) All digital input pins except pull-down/pull-up pins should not be allowed to float.
(6) A 2.2 µF capacitor must be connected to the VCOM pin.

10.2. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to PVDD, DVDD and TVDD1/2/3/4. PVDD and TVDD2/3 are supplied from analog supply in system, and TVDD1/4 and DVDD are supplied from digital supply in system. Power lines of PVDD and TVDD2/3 should be distributed separately, from the point with low impedance of regulators or other parts.
DVSS1/2/3/4 and PVSS must be connected to the same ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the AK4191.

10.3. System Clock Connections

AK4191 has clock divider and PLL. Because of that devices AK4191 can operate various audio systems, Network player, USB DAC, CD player and so on.

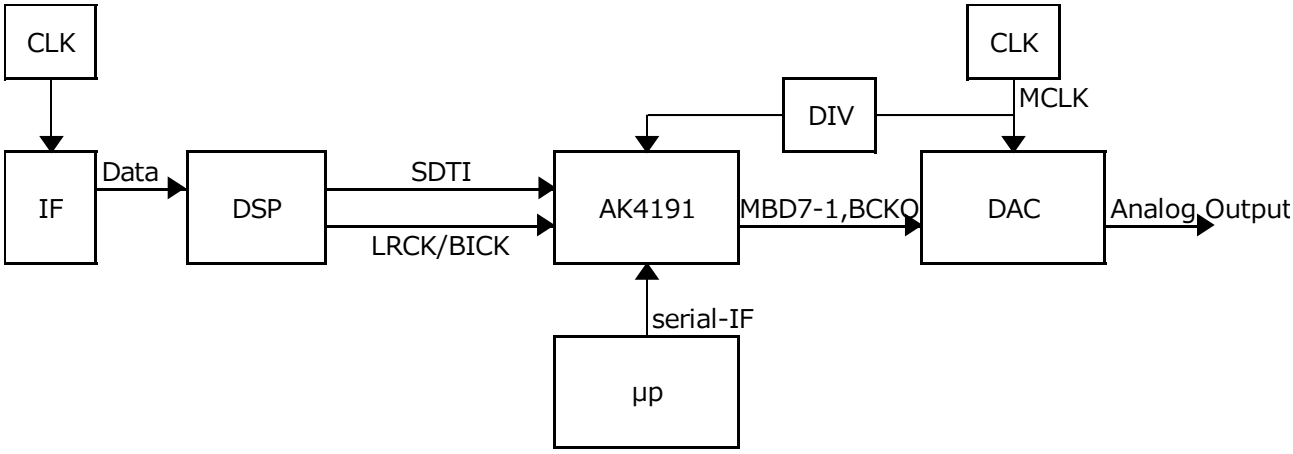


Figure 116. Asynchronous data is sent from audio source. MCLK is synchronized with data by AK4191.

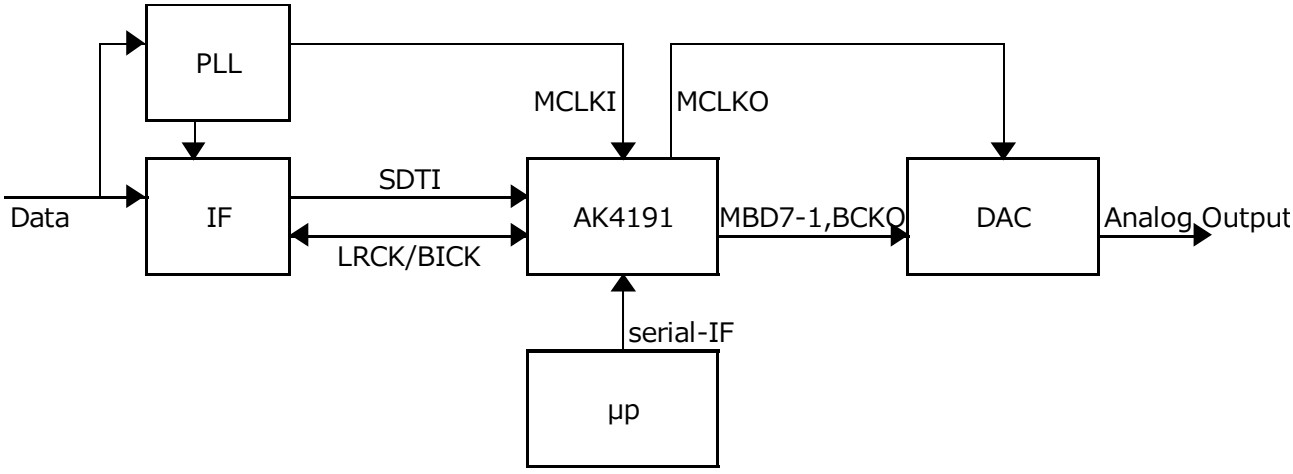
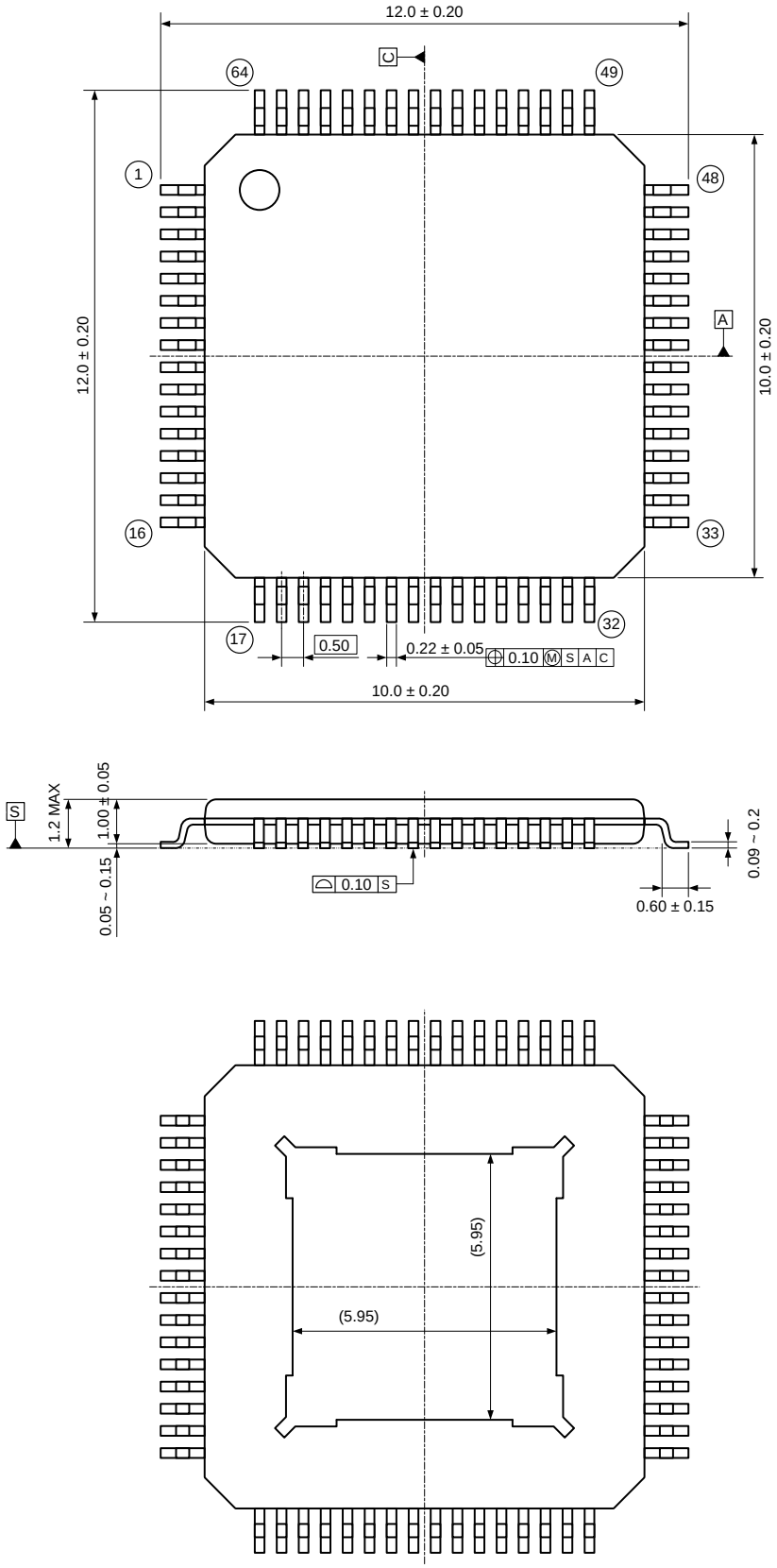


Figure 117. All devices are synchronized by audio data.

11. Package

11.1. Outline Dimensions: HTQFP64-10x10-0.5



-

11.2. Material & Terminal Finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	EFTEC-64T
Pin surface treatment:	Solder (Pb free) plate

11.3. Marking

1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4191EQ
4) AKM Logo

12. Ordering Guide

AK4191EQ	−40 to +85°C	64-pin HTQFP (0.5 mm pitch)
AKD4191	Evaluation Board for AK4191	

13. Revision Histroy

Date (Y/M/D)	Revision	Reason	Page	Contents
21/10/12	00	First Edition		
22/01/26	01	Error Collection	78	6.9 Digital Attenuator, Table 27 Transition time of 1 code shift →Transition time from setting 0dB to MUTE
		Error Collection	128	11.2 Lead frame material, EFTEC64→EFTEC-64T

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.

Rev.1