AK4499EX
Premium Switched Resistor Stereo DAC

1. General Description

The AK4499EX is a new concept Premium multi-bit Stereo DAC with newly developed Switched Resistor technology, achieving the industry's leading level low distortion and low noise characteristics. It is suitable for playback of high-resolution audio sources that are becoming widespread in Network Audio and USB-DACs Audio systems. Multi-bit Modulator input for a high-precision audio source playback.

Application: AV Receivers, CD/SACD player, Network Audios, USB DACs, USB Headphones, Measurement Equipment, Control Systems, Public Audios (PA)

2. Features

- **Stereo Switched Resistor DAC**
- **THD+N: -124 dB**
- **Dynamic Range, S/N: 138 dB (135 dB @Stereo)**
- **Multi-bit Modulator Data Interface with 5.6448, 11.2896 MHz Clock**
  - **7-bit Modulator Data**
- **Mono Mode**
- **Power Supply:**
  TVDD = DVDD to 3.6 V, DVDD = 1.7 to 1.98 V,
  AVDD = 4.75 to 5.25 V, VDDL/R = 4.75 to 5.25 V
- **Digital Input Level: CMOS**
- **Package: 64-pin HTQFP**
- **Temperature: -40 to 85 °C**

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4. Block Diagram and Functions

4.1. Block Diagram

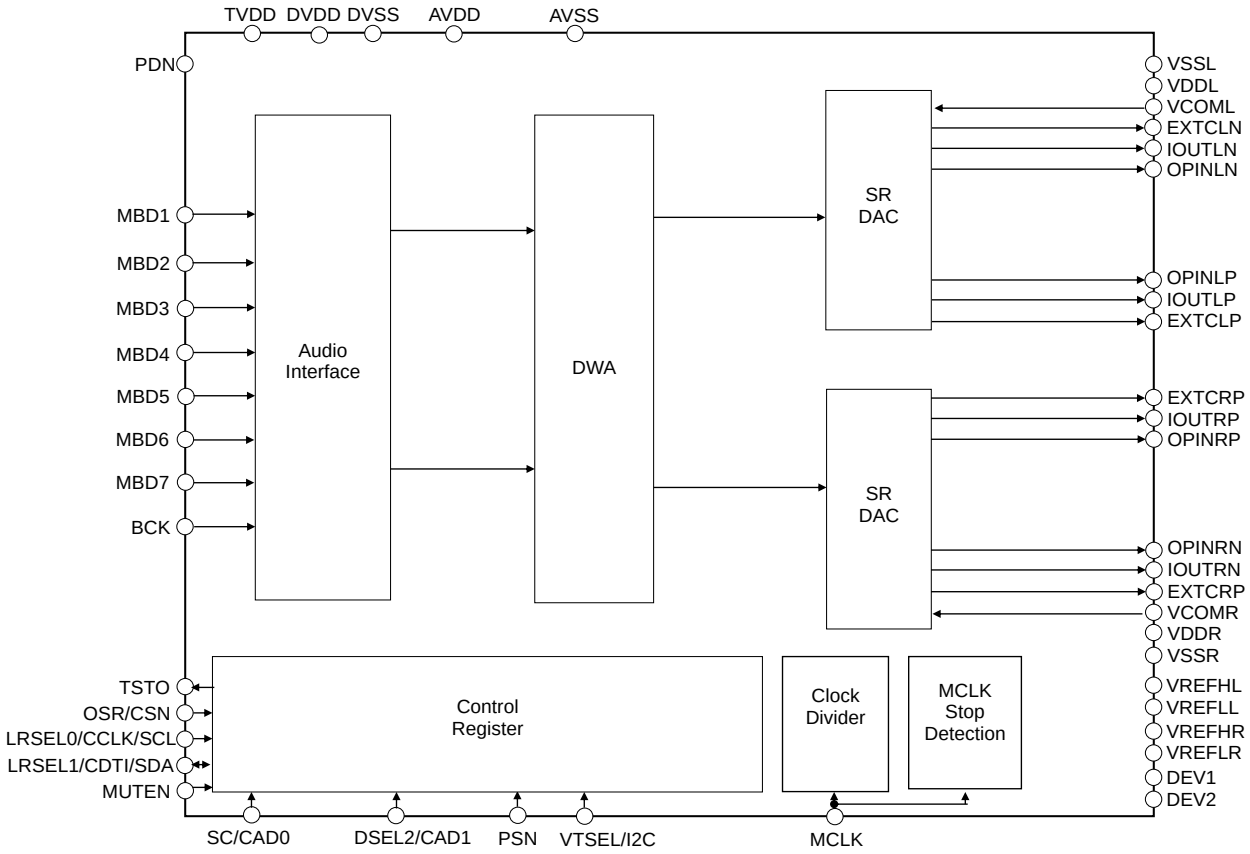


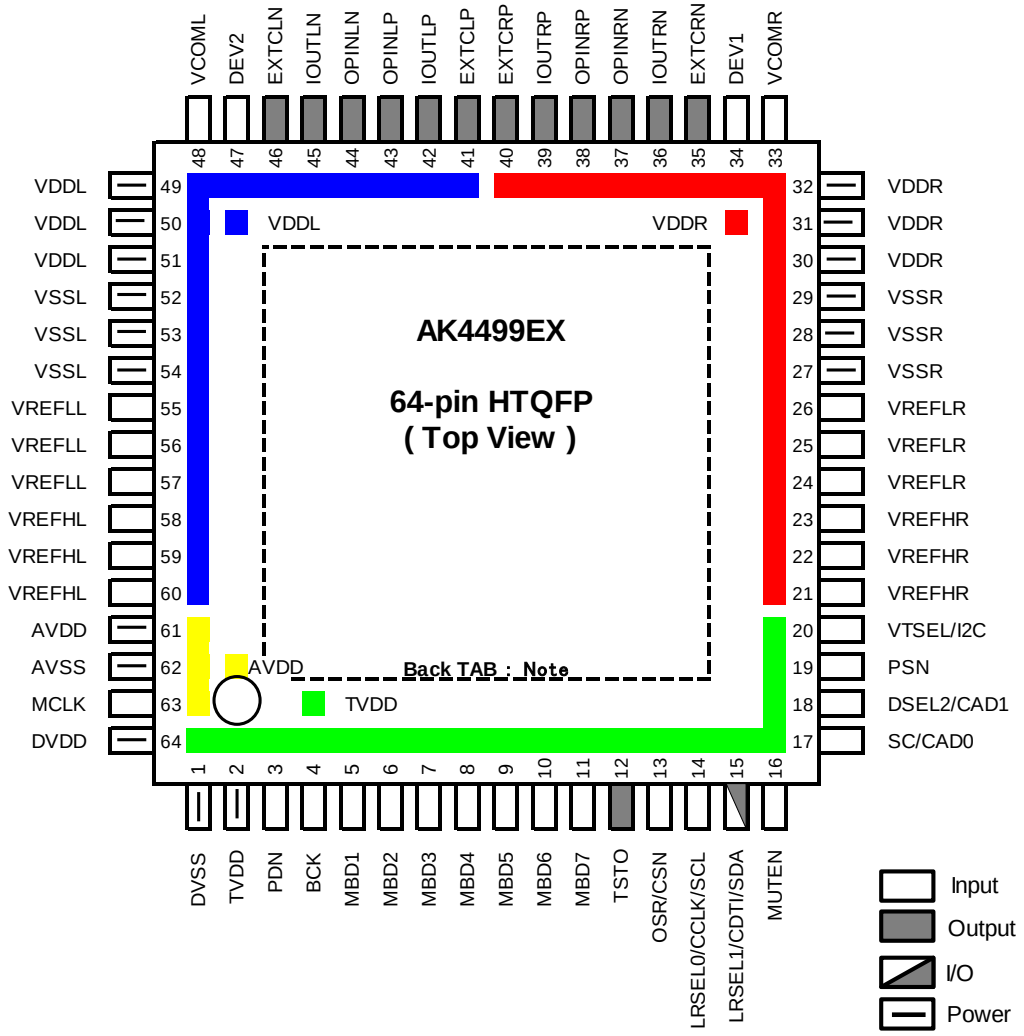
Figure 1. Block Diagram

4.2. Functions

Block	Functions
Audio Interface	BCK is used to clock MBD7-1 data into the shift register.
DWA	Processing two's complement MBD7-1 data by Data Weighted Average.
SR DAC	Converting MBD7-1 data from DWA output to analog signal and that is designed by Switched Resistor DAC.
Control Register	Internal registers keep its settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I^2C-Bus (SCL, SDA) control mode.
Clock Divider	Generates the clock for SR DAC from the input clock of the MCLK pin.
MCLK Stop Detection	Detects when the master clock input is absent.

5. Pin Configurations and Functions

5.1. Pin Configurations



Note. The exposed pad on the bottom surface of the package must be connected to ground.

5.2. Pin Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
1	DVSS	-	-	Digital Ground Pin.	-
2	TVDD	-		Digital Power Supply Pin, DVDD to 3.6 V.	-
3	PDN	I	TVDD/DVSS	Power Up, Power Down Pin. When at "L", the AK4499EX is in power down state and is held in reset. The AK4499EX must always be reset upon power up.	Hi-Z (PDN = "L")
4	BCK	I	TVDD/DVSS	Multi-Bit Data Clock Pin.	Hi-Z
5	MBD1	I	TVDD/DVSS	Multi-Bit Data1 Input Pin.	Hi-Z
6	MBD2	I	TVDD/DVSS	Multi-Bit Data2 Input Pin.	Hi-Z
7	MBD3	I	TVDD/DVSS	Multi-Bit Data3 Input Pin.	Hi-Z
8	MBD4	I	TVDD/DVSS	Multi-Bit Data4 Input Pin.	Hi-Z
9	MBD5	I	TVDD/DVSS	Multi-Bit Data5 Input Pin.	Hi-Z
10	MBD6	I	TVDD/DVSS	Multi-Bit Data6 Input Pin.	Hi-Z
11	MBD7	I	TVDD/DVSS	Multi-Bit Data7 Input Pin.	Hi-Z
12	TSTO	O	TVDD/DVSS	Test Output Pin.	Hi-Z
13	OSR	I	TVDD/DVSS	PSN pin = "H": Sampling Speed Mode Setting Pin in Pin Control mode. "L": OSR256 mode "H": OSR128 mode	Hi-Z
	CSN	I		PSN pin = "L", I2C pin = "L": Chip Select Pin in Register Control mode.	
14	LRSEL0	I	TVDD/DVSS	PSN pin = "H": Audio Interface Format Select and Data Select Pin in Pin Control mode.	Hi-Z
	CCLK	I		PSN pin = "L", I2C pin = "L": Control Data Clock Pin in Register Control mode.	
	SCL	I		PSN pin = "L", I2C pin = "H": Control Data Clock Input Pin	
15	LRSEL1	I	TVDD/DVSS	PSN pin = "H": Audio Interface Format Select and Data Select Pin in Pin Control mode.	Hi-Z
	CDTI	I		PSN pin = "L", I2C pin = "L": Control Data Input Pin in Register Control mode.	
	SDA	I/O		PSN pin = "L", I2C pin = "H": Control Data Input Pin.	
16	MUTEN	I	TVDD/DVSS	Mute State Select Pin. "L": Mute "H": Normal Operation	Hi-Z
17	SC	I	TVDD/DVSS	PSN pin = "H": Sound Control in Pin Control mode. "L": Measurement mode "H": Sound quality mode	Hi-Z
	CAD0	I		PSN pin = "L": Chip Address 0 Pin in Register Control mode.	
18	DSEL2	I	TVDD/DVSS	PSN pin = "H": Test Input Pin. Connect to TVDD in Pin Control mode.	Hi-Z
	CAD1	I		PSN pin = "L": Chip Address 1 Pin in Register Control mode.	
19	PSN	I	TVDD/DVSS	Pin control mode or Register Control mode Select Pin. (Internal pull-up pin) "L": Register control mode "H": Pin Control mode	Pull-Up to TVDD (100 kΩ, typ.)

20	VTSEL	I	TVDD/DVSS	PSN pin = “H”: Digital input voltage level of MCLK select pin in Pin Control Mode. “L”: High Level = 1.36 V, Low Level = 0.34 V “H”: High Level = 2.2 V, Low Level = 0.8 V	Hi-Z
	I2C	I		PSN pin = “L”: Register Control Interface Select Pin in Register Control mode.	
21	VREFHR	I	VDDR/VSSR	Rch High Level Voltage Reference Input Pin.	Hi-Z
22	VREFHR	I	VDDR/VSSR		Hi-Z
23	VREFHR	I	VDDR/VSSR		Hi-Z
24	VREFLR	I	VDDR/VSSR	Rch Low Level Voltage Reference Input Pin.	Hi-Z
25	VREFLR	I	VDDR/VSSR		Hi-Z
26	VREFLR	I	VDDR/VSSR		Hi-Z
27	VSSR	-	-	Analog Ground Pin.	-
28	VSSR	-	-	Analog Ground Pin.	-
29	VSSR	-	-	Analog Ground Pin.	-
30	VDDR	-	-	Rch Analog Power Supply 5.0 V(typ.) Pin.	-
31	VDDR	-	-	Rch Analog Power Supply 5.0 V(typ.) Pin.	-
32	VDDR	-	-	Rch Analog Power Supply 5.0 V(typ.) Pin.	-
33	VCOMR	I	VDDR/VSSR	Rch VCOM pin. VCOMR is connected to the midpoint of resistors between VREFHR and VREFLR.	Hi-Z
34	DEV1	I	VDDR/VSSR	Input Pin. Connect to Analog Ground. There is a Bidirectional Diode between DEV1 and VSSR.	Bidirectional diode to VSSR
35	EXTCRN	O	VDDR/VSSR	External Capacitor Connect Pin. This Pin should be connected to 1 µF to VSSR. (Internal pull-down pin)	Pull-Down to VSSR (250 kΩ, typ.)
36	IOUTRN	O	VDDR/VSSR	Current Output Pin. (Rch Negative Signal)	Connected to OPINRN (30 Ω, typ.)
37	OPINRN	O	VDDR/VSSR	Rch Negative Analog Signal Output pin. Connect to negative input pin of External OPAMP for I-V Conversion.	Connected to IOUTRN (30 Ω, typ.)
38	OPINRP	O	VDDR/VSSR	Rch Positive Analog Signal Output pin. Connect to negative input pin of External OPAMP for I-V Conversion.	Connected to IOUTRP (30 Ω, typ.)
39	IOUTRP	O	VDDR/VSSR	Current Output Pin. (Rch Positive Signal)	Connected to OPINRP (30 Ω, typ.)
40	EXTCRP	O	VDDR/VSSR	External Capacitor Connect Pin. This Pin should be connected to 1 µF to VSSR. (Internal pull-down pin)	Pull-Down to VSSR (250 kΩ, typ.)

41	EXTCLP	O	VDDL/VSSL	External Capacitor Connect Pin. This Pin should be connected to 1 µF to VSSL. (Internal pull-down pin)	Pull-Down to VSSL (250 kΩ, typ.)
42	IOUTLP	O	VDDL/VSSL	Current Output Pin. (Lch Positive Signal)	Connected to OPINLP (30 Ω, typ.)
43	OPINLP	O	VDDL/VSSL	Lch Positive Analog Signal Output pin. Connect to negative input pin of External OPAMP for I-V Conversion.	Connected to IOUTLP (30 Ω, typ.)
44	OPINLN	O	VDDL/VSSL	Lch Negative Analog Signal Output pin. Connect to negative input pin of External OPAMP for I-V Conversion.	Connected to IOUTLN (30 Ω, typ.)
45	IOUTLN	O	VDDL/VSSL	Current Output Pin. (Lch Negative Signal)	Connected to OPINLN (30 Ω, typ.)
46	EXTCLN	O	VDDL/VSSL	External Capacitor Connect Pin. This Pin should be connected to 1 µF to VSSL. (Internal pull-down pin)	Pull-Down to VSSL (250 kΩ, typ.)
47	DEV2	I	VDDL/VSSL	Input Pin. Connect to Analog Ground. There is a Bidirectional Diode between DEV2 and VSSL.	Bidirectional diode to VSSL
48	VCOML	I	VDDL/VSSL	Lch VCOM pin. VCOML is connected to the midpoint of resistors between VREFHL and VREFLL.	Hi-Z
49	VDDL	-	-	Lch Analog Power Supply 5.0 V(typ.) Pin.	-
50	VDDL	-	-	Lch Analog Power Supply 5.0 V(typ.) Pin.	-
51	VDDL	-	-	Lch Analog Power Supply 5.0 V(typ.) Pin.	-
52	VSSL	-	-	Analog Ground Pin.	-
53	VSSL	-	-	Analog Ground Pin.	-
54	VSSL	-	-	Analog Ground Pin.	-
55	VREFLL	I	VDDL/VSSL	Lch Low Level Voltage Reference Input Pin.	Hi-Z
56	VREFLL	I	VDDL/VSSL		Hi-Z
57	VREFLL	I	VDDL/VSSL		Hi-Z
58	VREFHL	I	VDDL/VSSL	Lch High Level Voltage Reference Input Pin.	Hi-Z
59	VREFHL	I	VDDL/VSSL		Hi-Z
60	VREFHL	I	VDDL/VSSL		Hi-Z
61	AVDD	-	-	Analog Power Supply 5.0 V(typ.) Pin.	-
62	AVSS	-	-	Analog Ground Pin.	-
63	MCLK	I	AVDD/AVSS	Master Clock Input Pin.	Hi-Z
64	DVDD	-	-	1.8 V(typ.) Power Supply Pin.	-
-	TAB	-	-	The TAB on the bottom surface of the package should be connected to Ground.	-

Note 1. All input pins except internal pull-up pins must not be left floating.
Note 2. The AK4499EX must be powered down by the PDN pin when changing Pin Control mode or Register Control mode by the PSN pin.

5.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Pin Control mode

Classification	Pin Name	Setting
Analog	IOUTLP, IOUTLN, OPINLP, OPINLN IOUTRP, IOUTRN, OPINRP, OPINRN	Open
Digital	TSTO	Open

Register Control mode (3-wire Serial Control Mode)

Classification	Pin Name	Setting
Analog	IOUTLP, IOUTLN, OPINLP, OPINLN IOUTRP, IOUTRN, OPINRP, OPINRN	Open
Digital	TSTO	Open

Register Control mode (I^2C-Bus Control Mode)

Classification	Pin Name	Setting
Analog	IOUTLP, IOUTLN, OPINLP, OPINLN IOUTRP, IOUTRN, OPINRP, OPINRN	Open
Digital	TSTO	Open
	CSN	Connect to DVSS

5.4. Pull-up, Pull-down Pin List

Classification	Pin name	Internal connection
Pull-up pin (Typ. = 100 kΩ)	PSN	TVDD
Pull-down pin (Typ. = 250 kΩ)	EXTCLP, EXTCLN,	VSSL
	EXTCRP,EXTCRN	VSSR

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = 0 V; Note 3, Note 4)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital I/O	TVDD	-0.3	4.0	V
	Digital Core	DVDD	-0.3	2.35	V
	Clock Interface	AVDD	-0.3	5.55	V
	Analog	VDDL/R	-0.3	5.55	V
Power Supplies Differences	VSSL, VSSR, AVSS, DVSS	ΔGND	0	0.3	V
	VDDL, VDDR, AVDD	ΔVD	0	0.3	V
Reference Voltage	High VREF	VREFHL	-0.3	VDDL + 0.3 ≤ 5.55	V
		VREFHR	-0.3	VDDR + 0.3 ≤ 5.55	V
	Low VREF	VREFLL	-0.3	+0.3	V
		VREFLR	-0.3	+0.3	V
	Common Voltage	VCOML	-0.3	VDDL + 0.3 ≤ 5.55	V
		VCOMR	-0.3	VDDR + 0.3 ≤ 5.55	V
Input Current, Any Pin Except Power Supplies and Reference Voltage		IIN	-	±10	mA
Analog Output Voltage IOUTLP/LN/RP/RN, OPINLP/LN/RP/RN		VOUTA	-0.3	VDDL/R + 0.3 ≤ 5.55	V
Input Voltage DEV1, DEV2		VDEV	-0.3	+0.3	V
Digital Input Voltage		VIND	-0.3	TVDD + 0.3 ≤ 4.0	V
MCLK Input Voltage		VINMCLK	-0.3	AVDD + 0.3 ≤ 5.55	V
Ambient Temperature (Power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages with respect to ground.
Note 4. AVSS, DVSS, VSSL, VSSR and TAB must be connected to the ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed above the recommended operating voltage.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = 0 V; Note 3, Note 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital I/O	TVDD	DVDD	1.8/3.3	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Clock Interface	AVDD	4.75	5.0	5.25	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Reference Voltage	High VREF	VREFHL	VDDL - 0.5	-	VDDL	V
		VREFHR	VDDR - 0.5	-	VDDR	V
	Low VREF	VREFLL	-	VSSL	-	V
		VREFLR	-	VSSR	-	V
	Common Voltage	VCOML	-	(VREFHL + VREFLL)/2	-	V
		VCOMR	-	(VREFHR + VREFLR)/2	-	V

Note 5. VDDL, VDDR and AVDD must be connected to the same voltage line.
Note 6. VDDL/R must be supplied at the same time as or before VREFHL/R.
Note 7. Regarding external circuit power up sequence refers to 9.7. Power Up Sequence of External Operational Amplifier for I-V Conversion.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

8.1. Analog Characteristics

OSR128 mode (OSR pin = "H" or OSR bit = "1")

(Ta = 25 °C; TVDD = 1.8 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL/R = VREFHL/R = 5.0 V, VSSL/R = VREFLL/R = 0 V; VCOML/R = (VREFHL/R + VREFLL/R)/2; MCLK = 22.5792 MHz, Sampling Frequency = BCK = 5.6448 MHz; Measurement bandwidth = 20 Hz to 20 kHz; Signal Frequency = 1 kHz; Input Signal Level = 0.805 × Full-scale = 0 dBr (Note 8); External circuit Figure 31; SC pin = "L" or SC bit = "0"

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics (Note 9)						
THD (Note 10)	BW = 20 kHz	0 dBr	-	-124	-	dB
	BW = 40 kHz	0 dBr	-	-124	-	dB
	BW = 80 kHz	0 dBr	-	-124	-	dB
THD+N	BW = 20 kHz	0 dBr	-	-124	-	dB
		-60 dBr	-	-72	-	dB
	BW = 40 kHz	0 dBr	-	-121	-	dB
		-60 dBr	-	-69	-	dB
	BW = 80 kHz	0 dBr	-	-118	-	dB
		-60 dBr	-	-66	-	dB
Dynamic Range (-60 dBr; A-weighted)			-	135	-	dB
S/N (A-weighted) (Note 11)		Stereo mode	-	135	-	dB
		Mono mode (Note 12)	-	138	-	dB
Inter-channel Isolation (1 kHz)			110	120	-	dB
DC Accuracy						
Inter-channel Gain Mismatch			-	-	0.3	dB
Gain Drift			-	100	-	ppm/°C
Differential Output Current (IOUTP - IOUTN) (Note 13)			-	72.8	-	mApp
Center Current (Note 14)			-	0	-	mA
Load Capacitance (Analog Output Pins) (Note 15)			-	-	5	pF

Note 8. 0 dBr is defined as 0.805 times the level of a 7-bit full-scale in two's complement format.
Note 9. The AK4191 is used as the input source with DSMSEL[1:0] bits = "00" and OBIT[1:0] bits = "00".
Note 10. Absolute resistance error of subsequent stage circuits (Figure 31) recommended to be less than 0.1 % to meet specifications.
Note 11. 2's complement "0" signal input.
Note 12. External circuits shown in Figure 32 are used in Mono mode.
Note 13. When the input signal is 0 dBr, the output current can be calculated by the following formula:
IOUTL (Typ. @ 0 dBr) = (IOUTLP) - (IOUTLN) = 72.8 mApp × (VREFHL - VREFLL)/5.
IOUTR (Typ. @ 0 dBr) = (IOUTRP) - (IOUTRN) = 72.8 mApp × (VREFHR - VREFLR)/5.
Note 14. Center current is the current that flows each IOUT pin during common output.
When positive input of operational amplifier in I-V Conversion = VCOML/R = (VREFHL/R + VREFLL/R)/2
Note 15. The load capacitance value of analog output pins (IOUTLP/LN/RP/RN pins, OPINLP/LN/RP/RN pins) is with respect to ground. The load capacitance should be as small as possible.

(Ta = 25 °C; TVDD = 1.8 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL/R = VREFHL/R = 5.0 V, VSSL/R = VREFLL/R = 0 V; VCOML/R = (VREFHL/R + VREFLL/R)/2; MCLK = 22.5792 MHz, Sampling Frequency = BCK = 5.6448 MHz; Measurement bandwidth = 20 Hz to 20 kHz; Signal Frequency = 1 kHz; Input Signal Level = 0.805 × Full-scale = 0 dBr (Note 8); External circuit Figure 31

Power Supplies					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current					
	Normal operation (PDN pin = “H”)				
	VDDL + VDDR (Note 16)	- -	12 (16)	-	mA mA
	VREFHL + VREFHR	-	46	-	mA
	AVDD	-	2	-	mA
	TVDD	-	0.1	-	mA
	DVDD	-	2	-	mA
	Total power dissipation VDDL/R + VREFHL/R + AVDD + TVDD + DVDD	-	308	-	mW
	Power down (PDN pin = “L”) (Note 17) VDDL/R + VREFHL/R + AVDD + TVDD + DVDD	-	10	150	µA
	Standby (Note 18) VDDL/R + VREFHL/R + AVDD + TVDD + DVDD	-	1000	-	µA

Note 16. The values in () at VDDL/R total power supply current indicate consumption current when there is zero input data.

Note 17. In power down state, the PSN pin = TVDD and all other digital input pins including clock pins (MCLK, BCK) are connected to DVSS.

Note 18. In the standby mode, the external clock (MCLK, BCK) is input, and the other digital input pins are connected to DVSS. The standby mode is set to STBY bit = “1” in the register control mode.

OSR256 mode (OSR pin = "L" or OSR bit = "0")

(Ta = 25 °C; TVDD = 1.8 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL/R = VREFHL/R = 5.0 V, VSSL/R = VREFLL/R = 0 V; VCOML/R = (VREFHL/R + VREFLL/R)/2; MCLK = 22.5792 MHz, Sampling Frequency = BCK = 11.2896 MHz; Measurement bandwidth = 20 Hz to 20 kHz; Signal Frequency = 1 kHz; Input Signal Level = 0.805 × Full-scale = 0 dBr (Note 8); External circuit Figure 31; SC pin = "L" or SC bit = "0"

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics (Note 9)						
THD (Note 10)	BW = 20 kHz	0 dBr	-	-116	-	dB
	BW = 40 kHz	0 dBr	-	-116	-	dB
	BW = 80 kHz	0 dBr	-	-116	-	dB
THD+N	BW = 20 kHz	0 dBr	-	-116	-	dB
		-60 dBr	-	-71	-	dB
	BW = 40 kHz	0 dBr	-	-113	-	dB
		-60 dB	-	-68	-	dB
	BW = 80 kHz	0 dBr	-	-110	-	dB
		-60 dBr	-	-65	-	dB
Dynamic Range (-60 dBr; A-weighted)			-	134	-	dB
S/N (A-weighted) (Note 11)		Stereo mode	-	134	-	dB
		Mono mode (Note 12)	-	137	-	dB
Inter-channel Isolation (1 kHz)			-	120	-	dB
DC Accuracy						
Inter-channel Gain Mismatch			-	-	0.3	dB
Gain Drift			-	100	-	ppm/°C
Differential Output Current (IOUTP - IOUTN) (Note 13)			-	72.8	-	mApp
Center Current (Note 14)			-	0	-	mA
Load Capacitance (Analog Output Pins) (Note 15)			-	-	5	pF

(Ta = 25 °C; TVDD = 1.8 V, DVDD = 1.8 V, AVDD = 5.0 V, AVSS = DVSS = 0 V; VDDL/R = VREFHL/R = 5.0 V, VSSL/R = VREFLL/R = 0 V; VCOML/R = (VREFHL/R + VREFLL/R)/2; MCLK = 22.5792 MHz, Sampling Frequency = BCK = 11.2896 MHz; Measurement bandwidth = 20 Hz to 20 kHz; Signal Frequency = 1 kHz; Input Signal Level = 0.805 × Full-scale = 0 dBr (Note 8); External circuit Figure 31

Power Supplies					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current					
Normal operation (PDN pin = “H”)					
	VDDL+VDDR (Note 16) VDDL+VDDR (Note 16)	- -	18 (24)	-	mA mA
	VREFHL+VREFHR	-	46	-	mA
	AVDD	-	3	-	mA
	TVDD	-	0.1	-	mA
	DVDD	-	4	-	mA
Total power dissipation VDDL/R + VREFHL/R + AVDD + TVDD + DVDD		-	343	-	mW
Power down (PDN pin = “L”) (Note 17) VDDL/R + VREFHL/R + AVDD + TVDD + DVDD		-	10	150	µA
Standby (Note 18) VDDL/R + VREFHL/R + AVDD + TVDD + DVDD		-	1000	-	µA

8.2. DC Characteristics

(Ta = -40 to 85 °C; VDDL/R = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = DVDD to 3.6 V, DVDD = 1.7 to 1.98 V; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK pin (Note 19) (VTSEL pin = "L" or VTSEL bit = "0") High-Level Input Voltage Low-Level Input Voltage	 VIHCK VILCK	 1.36 -	 - -	 - 0.34	 V V
MCLK pin (Note 19) (VTSEL pin = "H" or VTSEL bit = "1") High-Level Input Voltage Low-Level Input Voltage	 VIHCK VILCK	 2.2 -	 - -	 - 0.8	 V V
1.7 V ≤ TVDD < 3.0 V (except MCLK pin) High-Level Input Voltage Low-Level Input Voltage	 VIH VIL	 80 %TVDD -	 - -	 - 20 %TVDD	 V V
3.0 V ≤ TVDD ≤ 3.6 V (except MCLK pin) High-Level Input Voltage Low-Level Input Voltage	 VIH VIL	 70 %TVDD -	 - -	 - 30 %TVDD	 V V
Low-Level Output Voltage (SDA pin, 2.0 V < TVDD ≤ 3.6 V: Iout = 3 mA) (SDA pin, 1.7 V ≤ TVDD ≤ 2.0 V: Iout = 3 mA)	 VOL VOL	 - -	 - -	 0.4 20%TVDD	 V V
Input Leakage Current (Note 20)	Iin	-10	-	+10	μA

Note 19. The VTSEL pin should be changed while the PDN pin is "L", and VTSEL bit should be changed while STBY bit = "1", MCLK is stopped with MSTBYN bit = "0", MUTEN pin = "L" or MUTEN bit = "0".

Note 20. The PSN pin has internal pull-up resistors. Therefore, the PSN pin is not included in this specification.

8.3. Switching Characteristics

(Ta = -40 to 85 °C; VDDL/R = 4.75 to 5.25 V, AVDD = 4.75 to 5.25 V, TVDD = DVDD to 3.6 V, DVDD = 1.7 to 1.98 V, C_L = 20 pF)

Parameter	Symbol	Min.	Typ.	Max	Unit
Master Clock Timing, 11.2896MHz (typ.)					
Frequency	fCLK	10	11.2896	13.824	MHz
Duty Cycle	dCLK	45	50	55	%
Master Clock Timing, 22.5792MHz (typ.)					
Frequency	fCLK	20	22.5792	27.648	MHz
Duty Cycle	dCLK	45	50	55	%
BCK Timing @ OSR pin = "H" or OSR bit = "1"					
Frequency	fBCK	5	5.6448	6.912	MHz
Duty Cycle	dBCK	45	50	55	%
BCK Timing @ OSR pin = "L" or OSR bit = "0"					
Frequency	fBCK	10	11.2896	13.824	MHz
Duty Cycle	dBCK	45	50	55	%
Frequency Ratio from MCLK to BCK @ OSR pin = "H" or OSR bit = "1"					
MCLK = 11.2896 MHz		-	2	-	-
MCLK = 22.5792 MHz		-	4	-	-
Frequency Ratio from MCLK to BCK @ OSR pin = "L" or OSR bit = "0"					
MCLK = 11.2896 MHz		-	1	-	-
MCLK = 22.5792 MHz		-	2	-	-
Multi-bit Audio Interface Timing					
Multi-bit Mono mode (STME bit = "0") (LRSEL1-0 pins = "HH")					
MBD7-1 Hold Time	tMBH	5	-	-	nsec
MBD7-1 Setup Time	tMBS	5	-	-	nsec
Multi-bit Stereo mode (STME bit = "1") (LRSEL1-0 pins = "LL", "LH", "HL")					
BCK Edge to MBD7-1	tBMD	-5	-	5	nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial Control Mode):					
CCLK Period	tCCK	200	-	-	nsec
CCLK Pulse Width Low	tCCKL	80	-	-	nsec
Pulse Width High	tCCKH	80	-	-	nsec
CDTI Setup Time	tCDS	40	-	-	nsec
CDTI Hold Time	tCDH	40	-	-	nsec
CSN "H" Time	tCSW	150	-	-	nsec
CSN "↓" to CCLK "↑"	tCSS	50	-	-	nsec
CCLK "↑" to CSN "↑"	tCSH	50	-	-	nsec
Control Interface Timing (I^2C-Bus Control Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μsec
Clock Low Time	tLOW	1.3	-	-	μsec
Clock High Time	tHIGH	0.6	-	-	μsec
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μsec
SDA Hold Time from SCL Falling (Note 21)	tHD:DAT	0	-	-	μsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μsec
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μsec
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μsec
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μsec
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	nsec
Capacitive load on bus	Cb	-	-	400	pF
Power down & Reset Timing (Note 22)					
PDN Accept Pulse Width	tAPD	600	-	-	nsec
PDN Reject Pulse Width	tRPD	-	-	30	nsec

Note 21. The data must be held for more than 300 nsec (the falling time of SCL).
Note 22. The PDN pin must be held "L" for more than 600 nsec to ensure a reliable reset.

8.4. Timing Diagram

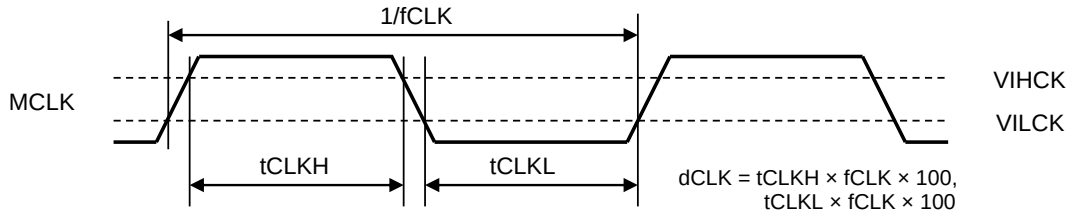


Figure 2. Clock Timing

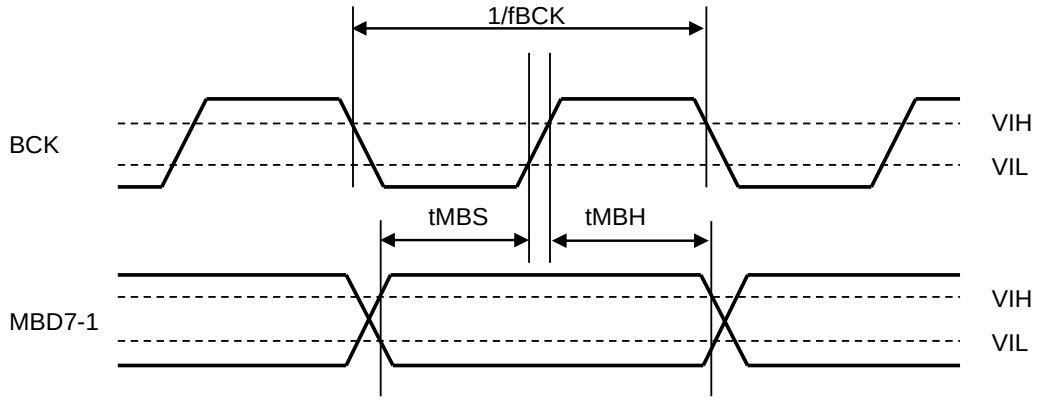


Figure 3. Audio Interface Timing
(Mono mode, STME bit = “0”, PSN pin = “L”, LRSEL1-0 pins = “HH”, PSN pin = “H”)

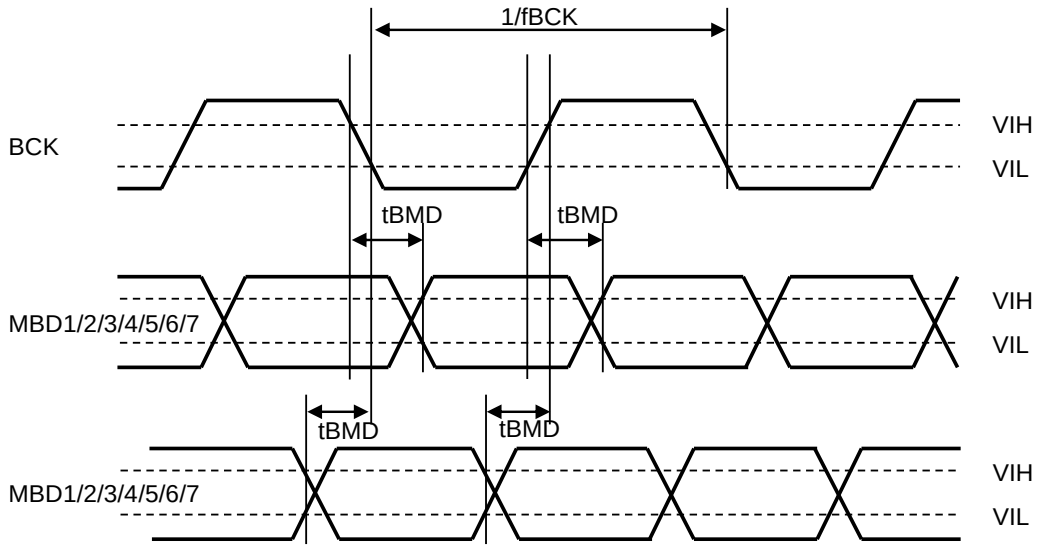


Figure 4. Audio Interface Timing
(Stereo mode, STME bit = “1”, PSN pin = “L”, LRSEL1-0 pins = “LL”, “LH”, “HL”, PSN pin = “H”)

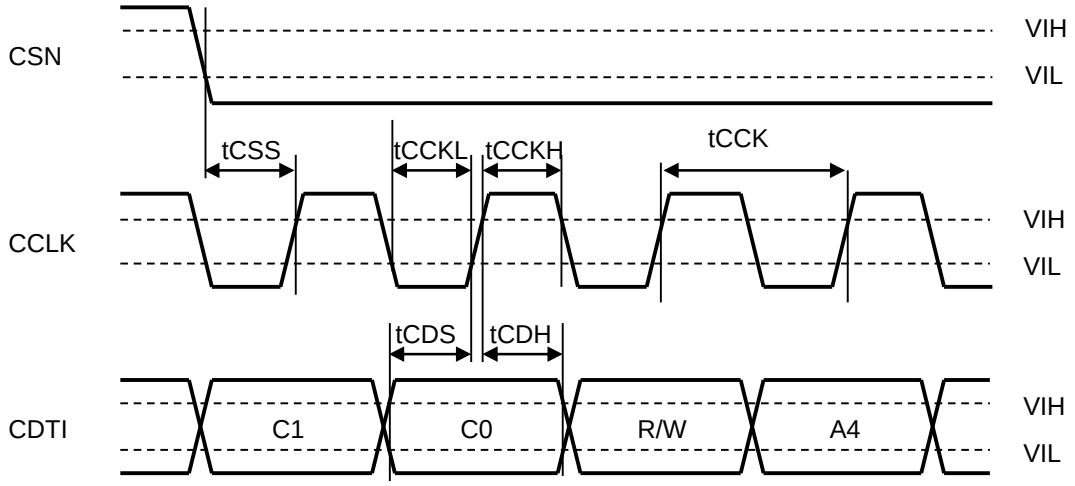


Figure 5. WRITE Command Input Timing

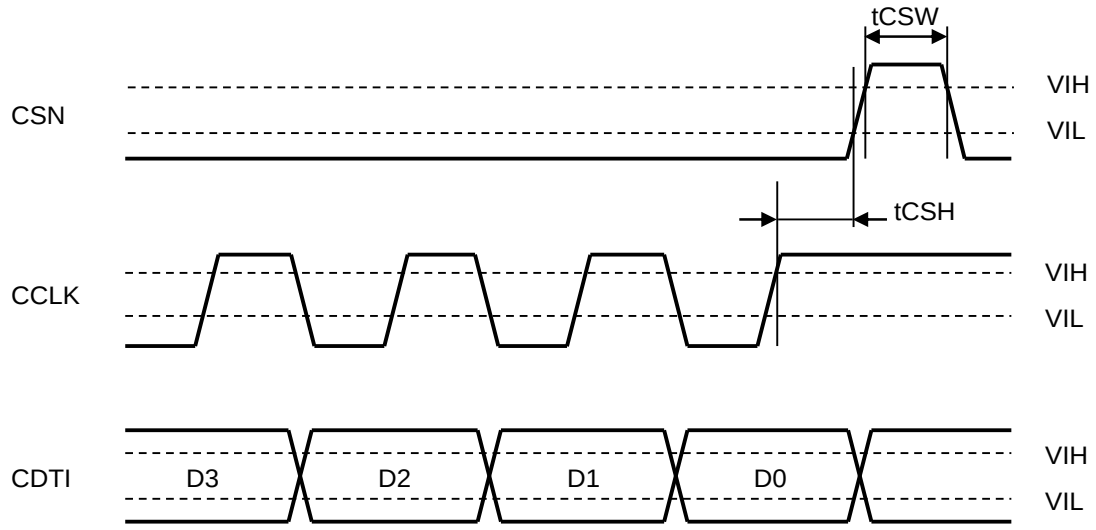


Figure 6. WRITE Data Input Timing

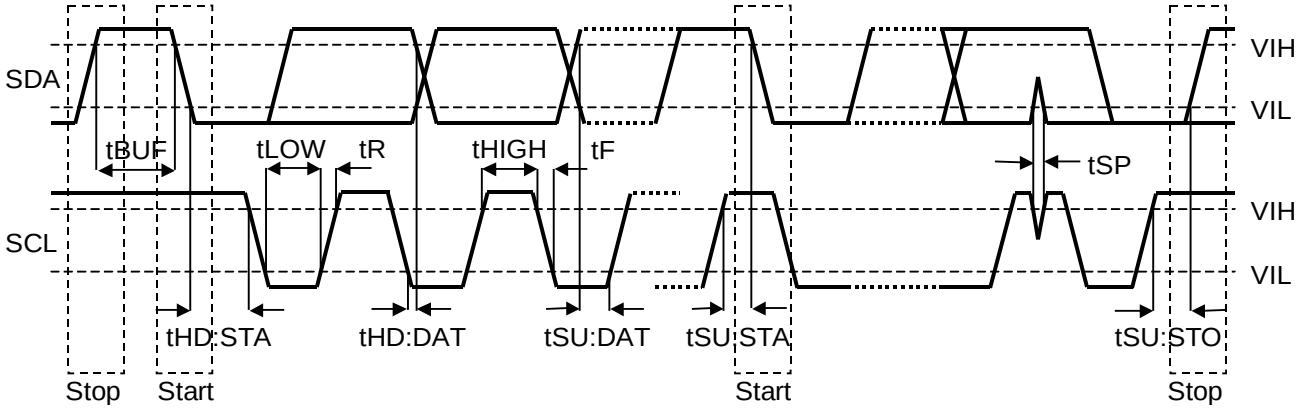


Figure 7. I²C-Bus mode Timing

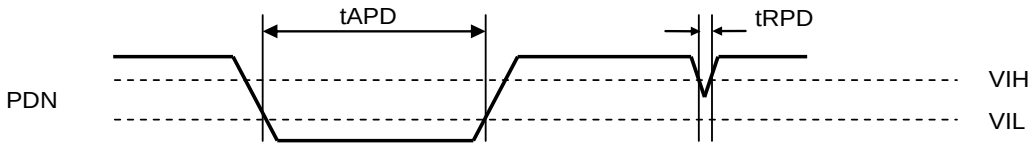


Figure 8. Power Down & Reset Timing

9. Functional Descriptions

Each function of the AK4499EX is controlled by pins (Pin Control mode) or registers (Register Control mode) (Table 1). Select the control mode by setting the PSN pin. The AK4499EX must be powered down by the PDN pin when changing the PSN pin setting. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not reinitialized.

Register settings are invalid in Pin Control mode, and pin settings are invalid in Register Control mode. Table 2 shows available functions of each control mode.

Table 1. Pin/Register Control Mode Select

PSN pin	Control Mode
L	Register Control mode
H	Pin Control mode

Table 2. Function List Pin/Register Control Mode

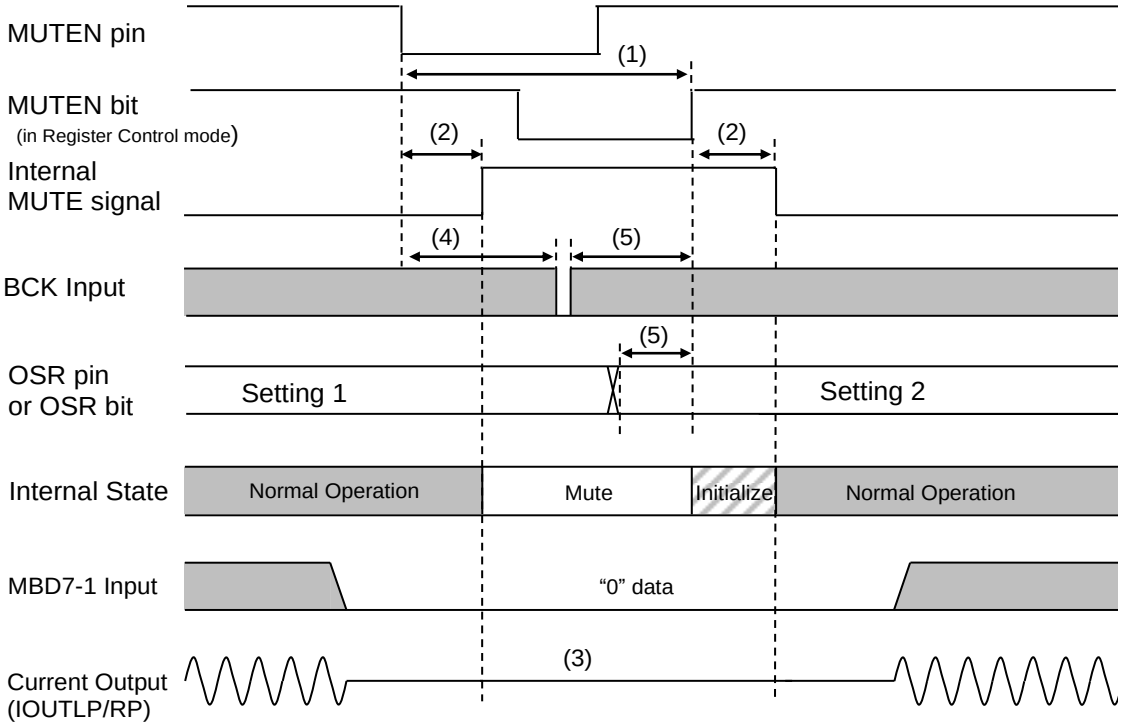
Function	Pin Control mode	Register Control mode
Operation rates select OSR256/OSR128	OSR pin	OSR bit
Stereo/Mono mode Select	LRSEL1-0 pins	STME bit
Output Signal Select		LSELN, RSELN bit
Sound Control	SC pin	SC bit
VIH/L level select of MCLK	VTSEL pin	VTSEL bit
Phase Inversion	Not available (Note 23)	INVL/R bit
On/off control of standby by MCLK	Not available (Note 24)	MSTBN bit
MUTE Function	MUTEN pin	MUTEN pin, MUTEN bit

Note 23. In Pin Control mode, the phase inversion function cannot be used.
Note 24. In Pin Control mode, the standby function by MCLK is forced ON.

9.1. Sampling Speed mode Setting

The AK4499EX has two sampling speed mode, such as OSR256 mode and OSR128 mode. The AK4499EX is set OSR256 mode when setting OSR pin = “L” or OSR bit = “0”, and it is set OSR128 mode when setting OSR pin = “H” or OSR bit = “1”.

In case the data sample rate is changed with OSR pin or bit, the AK4499EX should be mute by MUTEN pin or bit to prevent output the noise from the AK4499EX. OSR pin or bit should be changed more than 50 μsec later MUTEN pin or bit signal down edge. MUTEN pin or bit signal should be turned up at 50 μsec later OSR pin or bit fixed setting and BCK clock frequency changing.



Notes:

(1) Both MUTEN pin and MUTEN bit are enable in Register Control mode. The period of MUTEN pin = “L” or MUTEN bit = “0” must be 100 μsec or more continuously.

(2) It takes up to 77 μsec until the internal MUTE signal is changed when changing MUTEN pin or MUTEN bit.

(3) The AK4499EX output “0” data via Current Output pins (IOUTLP, IOUTLN, IOUTRP, IOUTRN) when the internal MUTE signal is “1”.

(4) MCLK frequecny should be changed more than 77 μsec later from setting MUTEN pin = “L” or MUTEN bit = “0”. This sequence avoids noisy data output caused by the frequency ratio of MCLK to BCK being out of the normal range.

(5) When MUTEN is released, the initialization sequence is executed. The period between the switching of the BCK clock frequency or OSR setting and the release of MUTEN pin or MUTEN bit is at least 50 μsec to execute the initialization sequence correctly.

Figure 9. OSR pin and bit setting sequence

9.2. System Clock

The external clocks, which are required to operate the AK4499EX, are MCLK and BCK. In OSR256 mode, the MCLK speed is same or twice against BCK speed. In OSR128 mode, the MCLK speed is twice or quadruple against BCK speed. The AK4499EX will detect the MCLK and BCK frequency ratio to generate the internal operation clock from MCLK automatically. The phase between MCLK and BCK is not critical. The frequency of operating SR DAC is same as that of BCK.

The frequency of MCLK should be changed in Power Down, Standby or Mute states. This sequence avoids noisy data output caused by the frequency ratio of MCLK to BCK being out of the normal range. Refer to 9.9.3. Mute Function for the detailed sequence.

The AK4499EX is automatically placed in standby state when MCLK is stopped for more than 1 μsec during a normal operation, and the analog output becomes floating state. When MCLK is input again, the AK4499EX exits standby state and starts operation. This standby function will be disable by setting MSTBN bit = "1" in Register Control mode. The AK4499EX is in power down state until MCLK and BCK are supplied, and the analog output is floating state when power down is released (PDN pin = "L" → "H").

Table 3. BCK, MCLK frequency and Sampling Speed Mode

OSR pin or OSR bit	Sampling Speed Mode	44.1 kHz base		48 kHz base		Frequency Ratio from MCLK to BCK
		BCK frequency	MCLK frequency	BCK frequency	MCLK frequency	
L or 0	OSR256	11.2896 MHz	11.2896 MHz	12.288 MHz	12.288 MHz	1
			22.5792 MHz		24.576 MHz	2
H or 1	OSR128	5.6448 MHz	11.2896 MHz	6.144MHz	12.288 MHz	2
			22.5792 MHz		24.576 MHz	4

9.3. Audio Inerface Format

Two audio interface format modes, such as Multi-bit Mono mode and Multi-bit Stereo mode, are selectable by using the LRSEL1-0 pins in Pin Control mode and STME bit in Register Control mode.

Table 4. Audio Interface Format Select (Pin Control mode)

LRSEL1 pin	LRSEL0 pin	Audio Interface Format
L	L	Multi-Bit Stereo
L	H	
H	L	
H	H	Multi-Bit Mono

Table 5. Audio Interface Format Select (Register Control mode)

STME bit	Audio Interface Format
0	Multi-Bit Mono
1	Multi-Bit Stereo

9.3.1. Multi-Bit Mono Interface mode (single channel mode, no adding)

In this mode, the AK4499EX receives one channel of audio data. The data is two's complement format, each of which must be input to the MBD7-1 pins in synchronizing to BCK. The data is read out the rising edge of BCK input. Figure 10 shows the data format in Multi-bit Mono mode. D0[7:1], D1[7:1], D2[7:1] and D3[7:1] in the figure are one channel data.

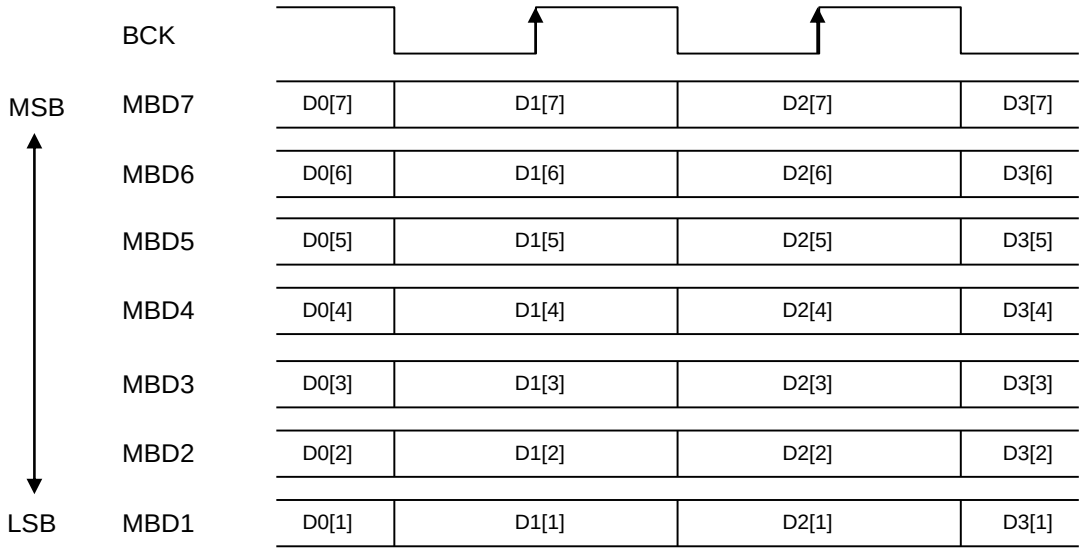


Figure 10. Multi-Bit Mono Interface mode

9.3.2. Multi-Bit Stereo Interface mode

In this mode, the AK4499EX receives stereo audio data. The data is two's complement format, each of which must be input to the MBD7-1 pins in synchronizing to BCK. The data is read out by the BCK input. Figure 11 shows the data format in Multi-bit Stereo mode. R0[7:1], L1[7:1], R1[7:1], L2[7:1], R2[7:1] and L3[7:1] in the figure are one channel data.

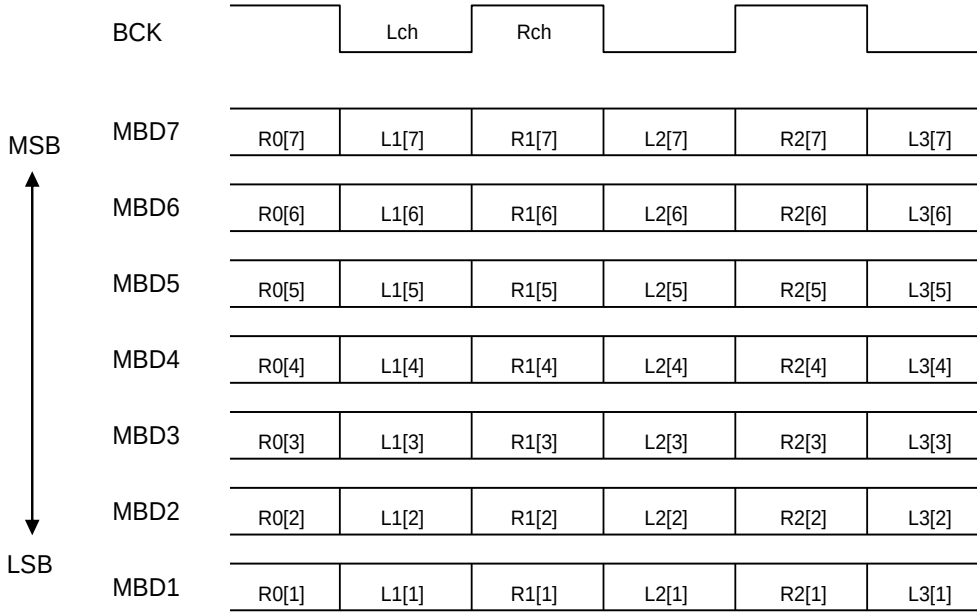


Figure 11. Multi-Bit Stereo Interface mode

9.4. Multi-Bit Interface Mode Select, Output Signal Select

(1) Register Control Mode (PSN pin = “L”)

Input and output combination of the AK4499EX can be changed by LSELN bit and RSELN bit (Table 6). These functions are available on Multi-bit Stereo Interface audio format (STME bit = “1”).

Table 6. Output Signal Selection (Register Control mode)

LSELN bit	RSELN bit	IOUTLP/N	IOUTRP/N	
0	0	Lch Input	Rch Input	(default)
0	1	Lch Input	Lch Input	
1	0	Rch Input	Rch Input	
1	1	Rch Input	Lch Input	

(2) Pin Control Mode (PSN pin = “H”)

Audio interface format mode and Input/output combination of the AK4499EX can be changed by the LRSEL1-0 pins (Table 7).

Table 7. Audio Interface Format and Output Signal Selection (Pin Control mode)

LRSEL1 pin	LRSEL0 pin	Audio Interface Format	Output Selection	
			IOUTLP/N	IOUTRP/N
L	L	Multi-Bit Stereo	Lch Input	Rch Input
L	H		Lch Input	Lch Input
H	L		Rch Input	Rch Input
H	H	Multi-Bit Mono	Mono Input	Mono Input

9.5. Phase Inversion Function (Register Control Mode)

The output signal phase can be inverted by INVL bit and INVR bit (Table 8).

Table 8. Phase Inversion Function

INVL bit	INVR bit	IOUTLP/N	IOUTRP/N	
0	0	Normal	Normal	(default)
0	1	Normal	Invert	
1	0	Invert	Normal	
1	1	Invert	Invert	

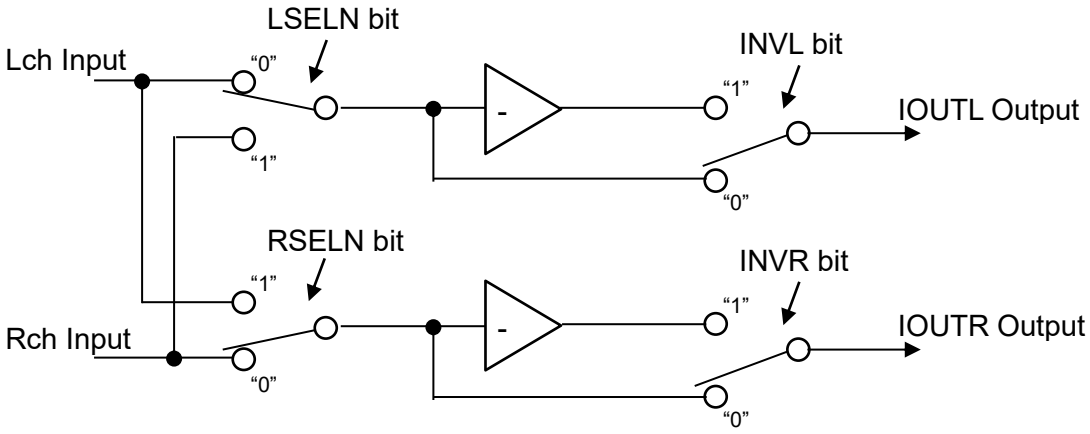


Figure 12. Output Signal Select and Phase Inversion Block Diagram

9.6. Sound Control

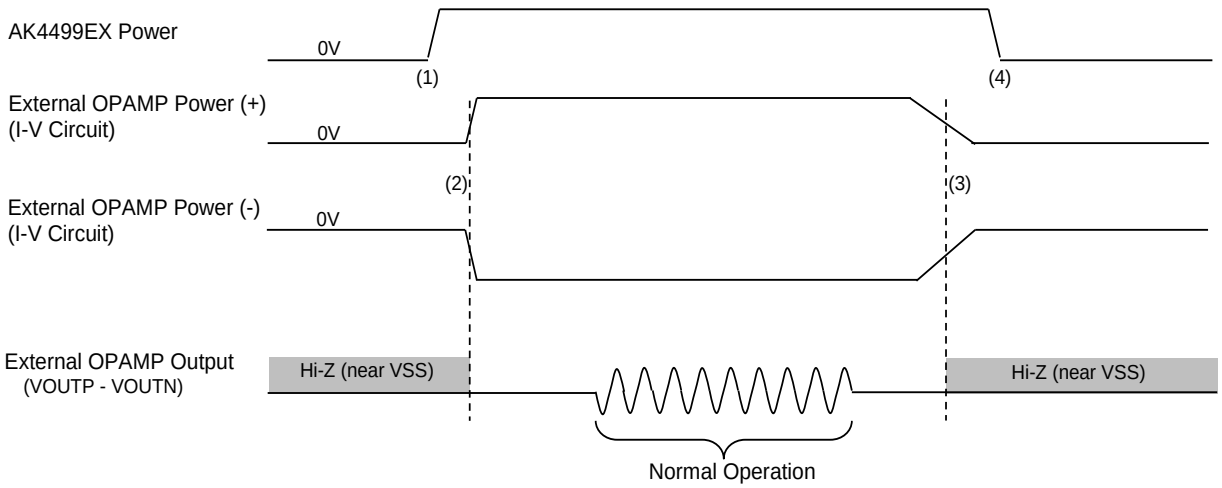
The AK4499EX has a function to control the sound quality by setting SC pin or SC bit (Table 9). The analog characteristics of the AK4499EX are specified in Setting 1, and the characteristics are not guaranteed at Setting 2.

Table 9. Sound Quality Select Mode

SC pin (bit)	Sound
L (0)	Measurement Mode (Setting 1)
H (1)	Sound Quality Mode (Setting 2)

9.7. Power Up Sequence of External Operational Amplifier for I-V Conversion

The output current of the AK4499EX is converted voltage by external I-V conversion circuit. The operational amplifier used in this I-V conversion circuit must be powered up or stopped while the AK4499EX is powered up. By doing this, a feedback path of the operational amplifier is maintained, and it can protect the AK4499EX from fatal damage caused by excessive voltage input.



Notes:

(1) Power up the AK4499EX. Refer to 9.8. Power Up/Down Function.
(2) Power up an external operational amplifier after power up the AK4499EX.
(3) When power down the system, the external amplifier must be powered down before the AK4499EX.
(4) Power down the AK4499EX after the external amplifier. Refer to 9.8. Power Up/Down Function.

Figure 13. Power Up Sequence of External Operational Amplifier for I-V Conversion

There is a possibility of IC destruction due to breakdown of the withstanding voltage of the analog output pins (IOUTLP/LN/RP/RN) if the power supply of the external operational amplifier is turned on before power up the AK4499EX. Therefore, connect a Zener diode (V_{RWM} = 6 to 7 V) between each VDDL/R and VSSL/R if the power up/down sequence shown in Figure 13 cannot be followed.

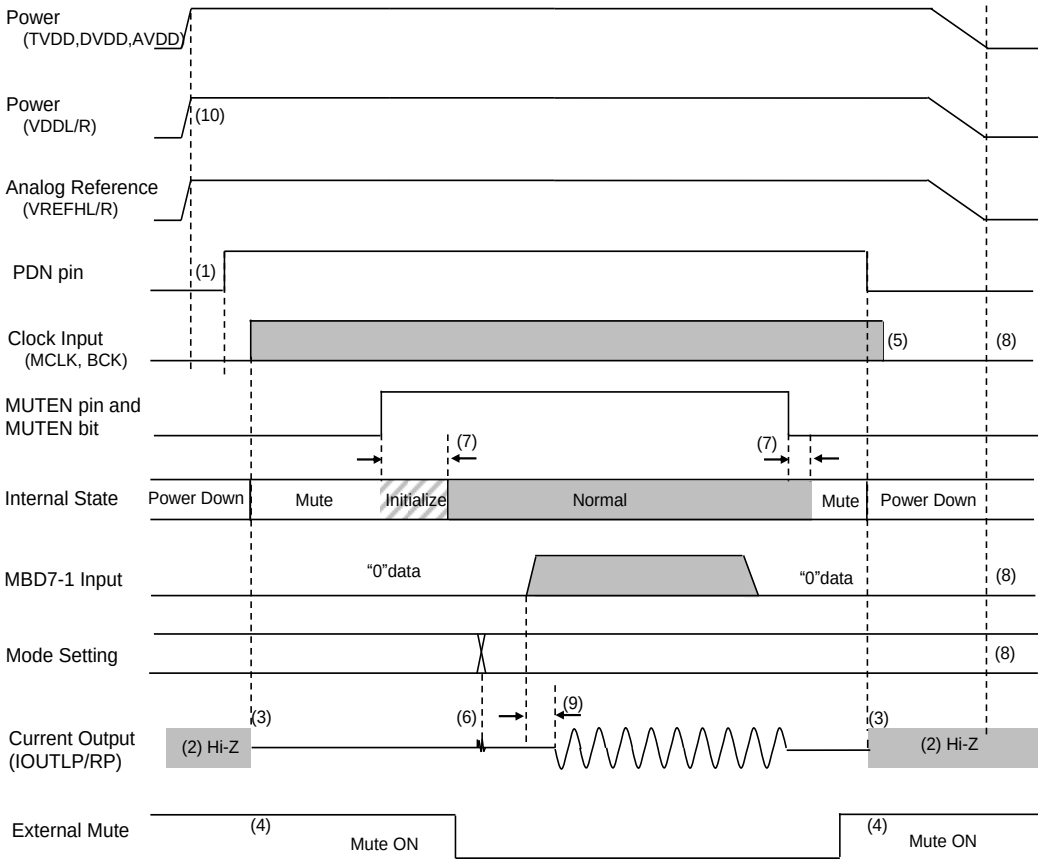
If the power supply of the external amplifier is turned on before power up the AK4499EX, there is a possibility that click noise occurs due to DC difference. Connect an external mute circuit to the analog signal line to prevent this click noise (Figure 35).

9.8. Power Up/Down Function

The AK4499EX is powered down by setting the PDN pin to “L”. In power down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-Z) state. The PDN pin must be held “L” for more than 600 nsec to ensure a reliable reset. There is a possibility of malfunctions with the “L” pulse less than 600 nsec. Power down is released by setting the PDN pin to “H” from “L”.

(1) Register Control mode (PSN pin = “L”)

The PDN pin = “H” and MSTBN bit = “0”, the AK4499EX is started to output analog signal by inputting MCLK. If the MSTBN bit is changed from “0” to “1” after the PDN pin sets to “H”, the analog outputs of the AK4499EX are “0” data outputs, not Hi-Z, even when MCLK is not supplied. After that all internal circuits are turned on and the AK4499EX is set in normal operating state, after the MUTEN pin = “H” and MUTEN bit = “1” is set and BCK is input. Figure 14 shows system timing example of power down/up.



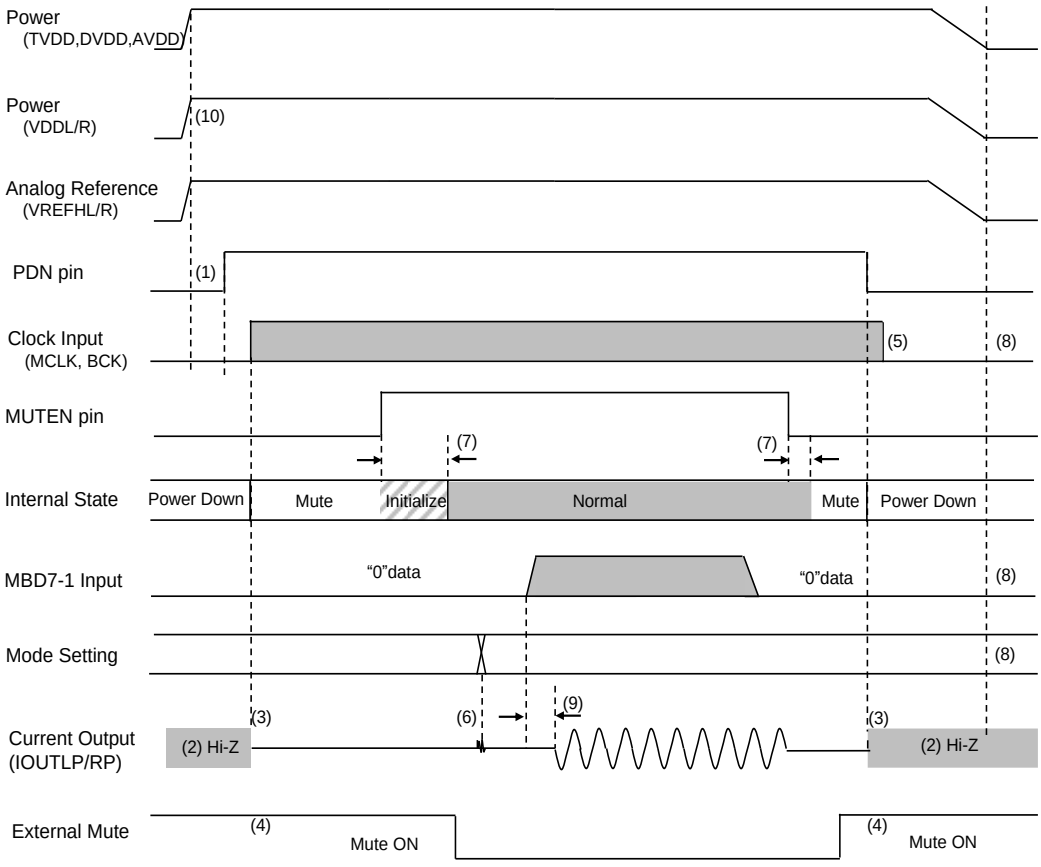
Notes:

(1) The PDN pin must be held “L” for more than 600 nsec after supplying TVDD, DVDD, AVDD and VDDL/R reached 90 %.
(2) Analog outputs are floating (Hi-Z) in power down state.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(4) Mute the analog output externally if click noise (3) adversely affect system performance.
(5) Clock inputs (MCLK and BCK) can be stopped in power down state.
(6) Click noise occurs at the edge of mode setting signals (LRSELN bit, LRSELN bit and SC bit). This noise is output even if “0” data is input.
(7) Setting MUTEN pin = “H” and MUTEN bit = “1”, it is available to output signal and all circuit is powered up. When MUTEN is released, the initialization sequence is executed. It takes up to 77 µsec until the internal MUTE signal is changed when changing MUTEN pin and MUTEN bit.
(8) Do not input all clocks, data and mode setting signals when power supplies are powered down.
(9) It takes about 7-BCK cycles to output the analog signal corresponding to the digital input.
(10) VDDL/R must be supplied at the same time as or before VREFHL/R.

Figure 14. Power up/down sequence example in Register Control mode

(2) Pin Control mode (PSN pin = “H”)

The PDN pin = “H”, the AK4499EX is started to output analog signal by inputting MCLK. After that all internal circuits are turned on and the AK4499EX is set in normal operating state, after the MUTEN pin = “H” is set and BCK is input. Figure 15 shows system timing example of power down/up.



Notes:

(1) The PDN pin must be held “L” for more than 600 nsec after supplying TVDD, DVDD, AVDD and VDDL/R reached 90 %.
(2) Analog outputs are floating (Hi-Z) in power down state.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(4) Mute the analog output externally if click noise (3) adversely affect system performance.
(5) Clock inputs (MCLK and BCK) can be stopped in power down state.
(6) Click noise occurs at the edge of mode setting signals (LRSEL0 pin, LRSEL1 pin and SC pin). This noise is output even if “0” data is input.
(7) Setting the MUTEN pin = “H”, it is available to output signal and all circuit is powered up. When MUTEN is released, the initialization sequence is executed. It takes up to 77 μsec until the internal MUTE signal is changed when changing the MUTEN pin.
(8) Do not input all clocks, data and mode setting signals when power supplies are powered down.
(9) It takes about 7-BCK cycles to output the analog signal corresponding to the digital input.
(10) VDDL/R must be supplied at the same time as or before VREFHL/R.

Figure 15. Power up/down sequence example in Pin Control mode

9.9. Internal State

The AK4499EX has five states shown in Table 10. Power Down, Standby and Mute states are controlled by PDN pin, STBY bit, MCLK input, MUTEN pin and MUTEN bit.

Table 10. Internal States

State	PDN pin	STBY bit	MCLK input	MUTEN pin (bit) (Note 26)	Audio Interface, DWA	SR DAC	IOUTLP/N, IOUTRP/N state
Power Down	L	- (*)	- (*)	- (*)	OFF	OFF	Hi-Z
Standby	H	1	- (*)	- (*)	OFF	OFF	Hi-Z
Standby (MCLK Stop) (Note 25)	H	0	Not Supplied	- (*)	OFF	OFF	Hi-Z
Mute	H	0	Supplied	L (0)	OFF	ON	“0” data
Normal Operation	H	0	Supplied	H (1)	ON	ON	Signal output

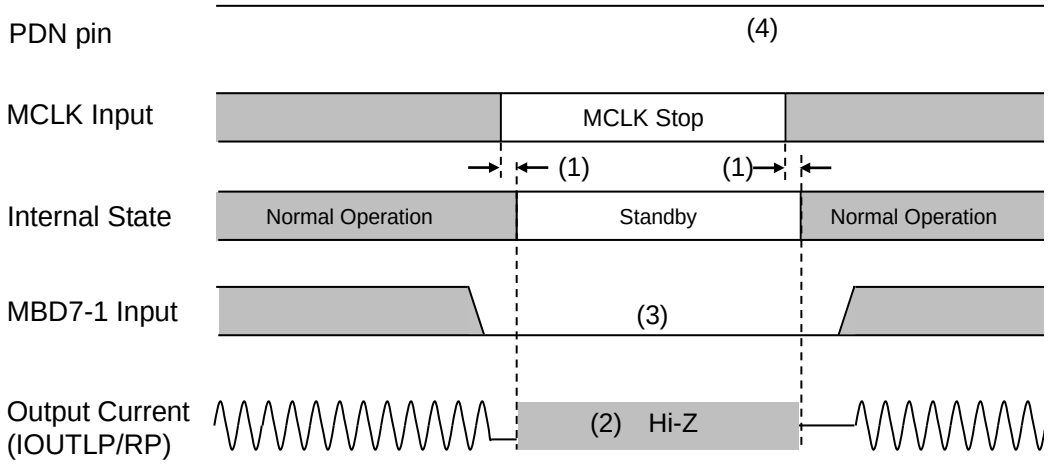
(*); - means “Do not care”

Note 25. In Register Control mode, this function is valid by MSTBN bit = “0” setting. Output pins and internal state depends on the PDN pin, STBY bit and the MUTEN pin setting, in case MSTBN bit = “1”.

Note 26. The internal state depends only on the setting of the MUTEN pin in Pin Control mode, and it depends on the setting of the MUTEN pin and MUTEN bit in Register Control mode (Table 11).

9.9.1. Standby Sequence by MCLK Input

The AK4499EX detects a clock stop and all circuits except MCLK stop detection circuit and Control Register stops operation if MCLK is not input for more than 1 μsec during operation (PDN pin = “H”). In this case, the analog output goes floating state (Hi-Z). The AK4499EX returns to normal operation after starting to supply MCLK again. This function is disabled to set MSTBN bit = “1” in Register Control mode.



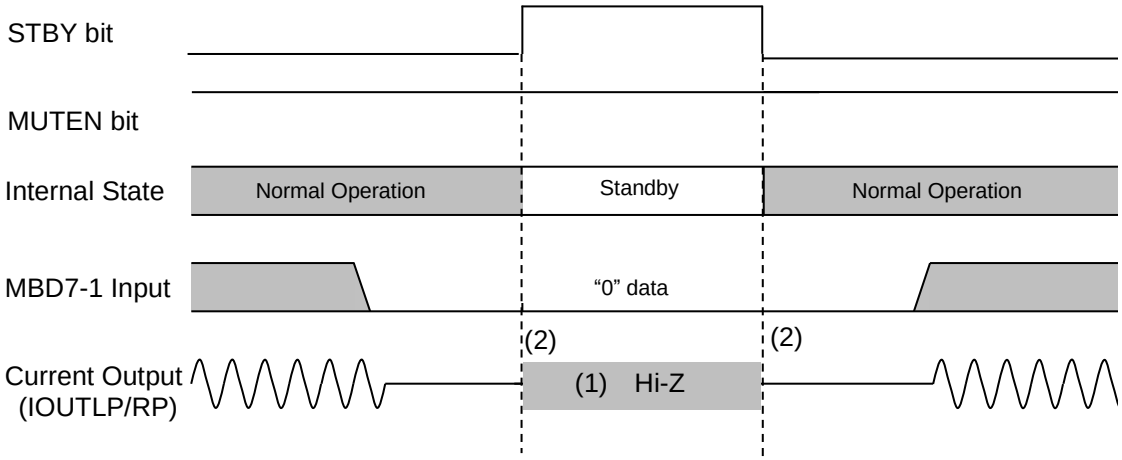
Notes:

(1) The AK4499EX detects MCLK stop and becomes standby state when MCLK edge is not detected for more than 1 μsec during operation.
(2) The analog output goes to floating state (Hi-Z).
(3) Click noise can be reduced by inputting “0” data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the standby state by MCLK. In this case, power up sequence by the PDN pin is not necessary.

Figure 16. Standby Sequence by MCLK Input

9.9.2. Standby Sequence by STBY bit

The AK4499EX is in standby by setting STBY bit. All circuits stop operation with STBY bit = “1” except MCLK stop detection, Control register and Clock divider circuits. In this case, the analog output becomes floating (Hi-Z). Figure 17 shows Standby sequence by Standby bit.



Notes:

(1) The analog output goes to floating state (Hi-Z), STBY bit = “1”.
(2) Click noise can be reduced by inputting “0” data.

Figure 17. Standby Sequence by STBY bit

9.9.3. Mute Function

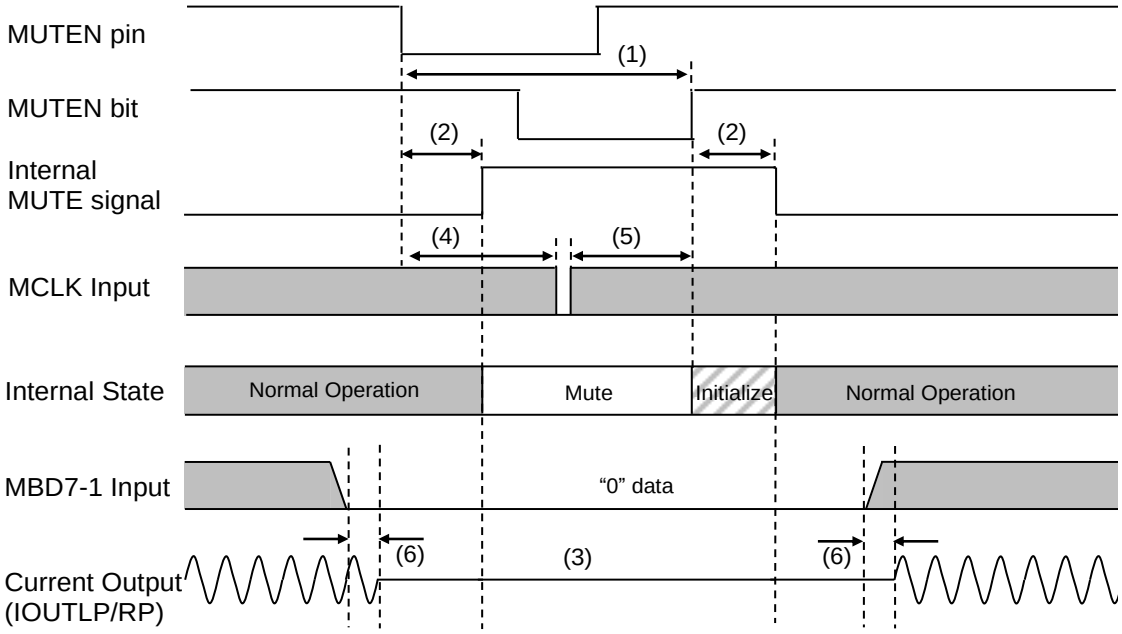
(1) Register Control mode (PSN pin = “L”)

MUTE function starts by the MUTEN pin = “L” or MUTEN bit =”0” in Register Control Mode. The mute state setting is as shown in Table 11.

Table 11. MUTE state setting

MUTEN pin	MUTEN bit	Operation
L	0	Mute
L	1	Mute
H	0	Mute
H	1	Normal Operation

Audio Interface and DWA are stopped by setting MUTEN pin to “L” or MUTEN bit to “0”, and the AK4499EX output “0” data via Current Output pins (IOUTLP, IOUTLN, IOUTRP, IOUTRN). Figure 18 shows Mute sequence by MUTEN pin and MUTEN bit.



Notes:

(1) Both MUTEN pin and MUTEN bit are enable in Register Control mode. The period of MUTEN pin = “L” or MUTEN bit = “0” must be 100 μsec or more continuously.

(2) It takes up to 77 μsec until the internal MUTE signal is changed when changing MUTEN pin and MUTEN bit.

(3) The AK4499EX output “0” data via Current Output pins (IOUTLP, IOUTLN, IOUTRP, IOUTRN) when the internal MUTE signal is “1”.

(4) MCLK frequency should be changed more than 77 μsec later from setting MUTEN pin = “L” or MUTEN bit = “0”. This sequence avoids noisy data output caused by the frequency ratio of MCLK to BCK being out of the normal range.

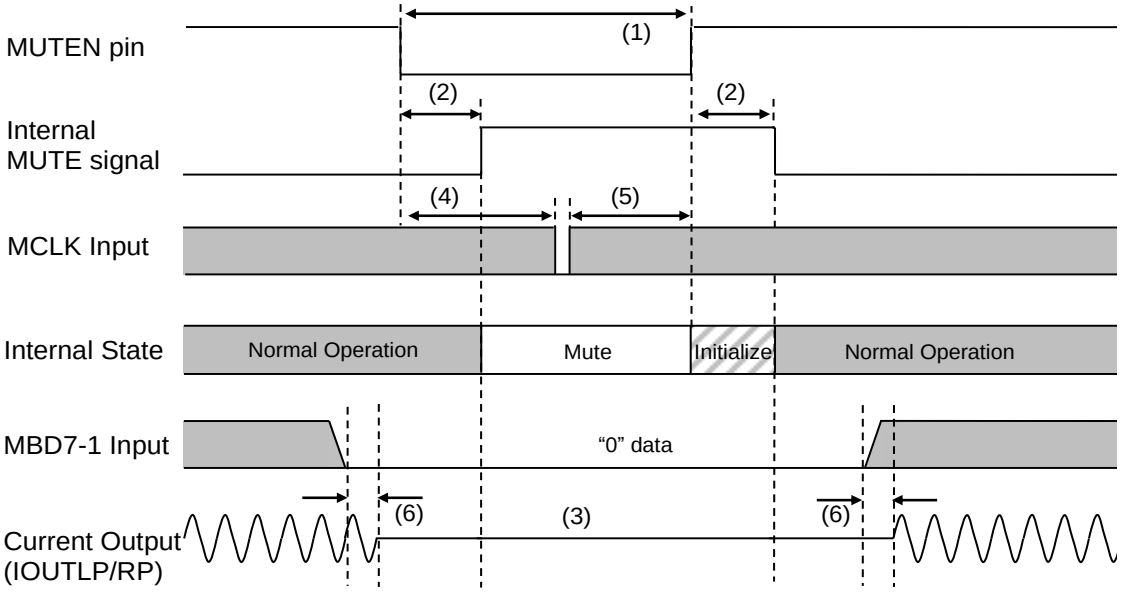
(5) When MUTEN is released, the initialization sequence is executed. The period between the switching of the clock frequency and the release of MUTEN pin or MUTEN bit is at least 50 μsec to execute the initialization sequence correctly.

(6) It takes about 7-BCK cycles to output the analog signal corresponding to the digital input.

Figure 18. Mute function in Register Control mode

(2) Pin Control mode (PSN pin= “H”)

Audio Interface and DWA are stopped by setting the MUTEN pin to “L”, and the AK4499EX output “0” data via Current Output pins (IOUTLP, IOUTLN, IOUTRP, IOUTRN). Figure 19 shows Mute sequence by the MUTEN pin.



Notes:

(1) The period of the MUTEN pin = “L” must be 100 μsec or more continuously.
(2) It takes up to 77 μsec until the internal MUTE signal is changed when changing the MUTEN pin.
(3) The AK4499EX output “0” data via Current Output pins (IOUTLP, IOUTLN, IOUTRP, IOUTRN) when the internal MUTE signal is “1”.
(4) MCLK frequency should be changed more than 77 μsec later from setting the MUTEN pin = “L”. This sequence avoids noisy data output caused by the frequency ratio of MCLK to BCK being out of the normal range.
(5) When MUTEN is released, the initialization sequence is executed. The period between the switching of the clock frequency and the release of the MUTEN pin is at least 50 μsec to execute the initialization sequence correctly.
(6) It takes about 7-BCK cycles to output the analog signal corresponding to the digital input.

Figure 19. Mute function in Pin Control mode

9.10. Register Control Interface

The AK4499EX has register control interface. This interface is enabled when the PDN pin is “H”. Control interface mode can be switched by the I2C pin (Table 12). The I2C pin should be set while the PDN pin is “L”. Setting the PDN pin to “L” resets the registers to their default values.

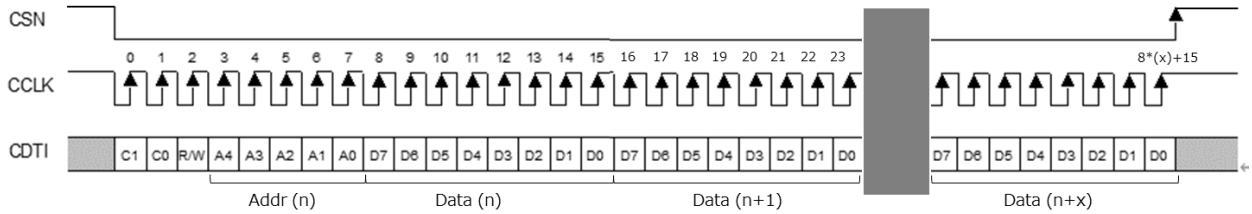
Table 12. Register Control Interface Mode Select

I2C pin	Mode
L	3-wire Serial Control Mode
H	I²C-Bus Control Mode

9.10.1. 3-wire Serial Control Mode (I2C pin = “L”)

Internal registers may be written to through 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bit, C1/0), Read/Write (1-bit; fixed to “1”, write only), Register address (MSB first, 5-bit) and Control data (MSB first, 8-bit). The data is output on a falling edge of CCLK, and the data is received on a rising edge of CCLK. Writing data is enabled by capturing D0. The maximum clock speed of CCLK is 5 MHz. If the address exceeds “02H”, the address counter will “roll over” to “00H” and the next write address will be “00H”.

Setting the PDN pin to “L” resets the registers to their default values.



C1-0 : Chip Address (C1 bit = CAD1 pin, C0 bit = CAD0 pin)
R/W : READ/WRITE (Fixed to “1”, Write only)
A4-0 : Register Address
D7-0 : Control Data

Figure 20. Control I/F Timing

Notes:
(1) The AK4499EX does not support read commands in 3-wire serial control mode.
(2) When the PDN pin = “L”, writing into control registers is prohibited.
(3) The control data cannot be written when the CCLK rising edge is 15 times or less during CSN is “L”

9.10.2. I²C-Bus Control Mode (I2C pin = "H")

The AK4499EX supports the fast-mode I²C-Bus.

(1) WRITE Operation

Figure 21 shows the data transfer sequence for the I²C-Bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 27). After the START condition, a slave address is sent. This address is seven bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 22). If the slave address matches that of the AK4499EX, the AK4499EX generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 28). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4499EX, and the format is MSB first. The most significant three bits are fixed as "000" (Figure 23). The data after the second byte contains control data. The format is MSB first, 8-bit (Figure 24). The AK4499EX generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 27).

The AK4499EX can perform more than one byte write operation per sequence. After receipt of the third byte the AK4499EX generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet, the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "02H" prior to generating a stop condition, the address counter will "roll over" to "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 29) except for the START and STOP conditions.

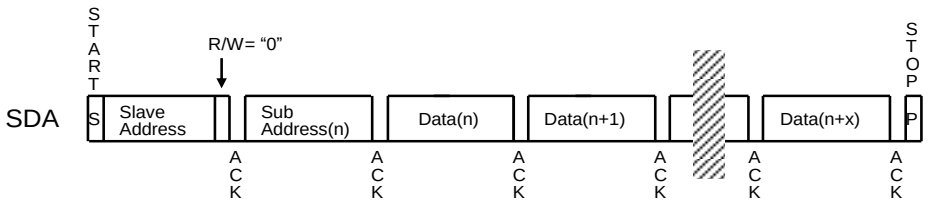


Figure 21. Data Transfer Sequence in I²C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1 and CAD0 are set by pin)

Figure 22. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 23. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 24. Byte Structure after The Second Byte

(2) READ Operation

Set the R/W bit = “1” for the READ operation of the AK4499EX. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet, the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “02H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4499EX supports two basic read operations: Current Address Read and Random Address Read.

(2)-1 Current Address Read

The AK4499EX has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4499EX generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4499EX ceases the transmission.

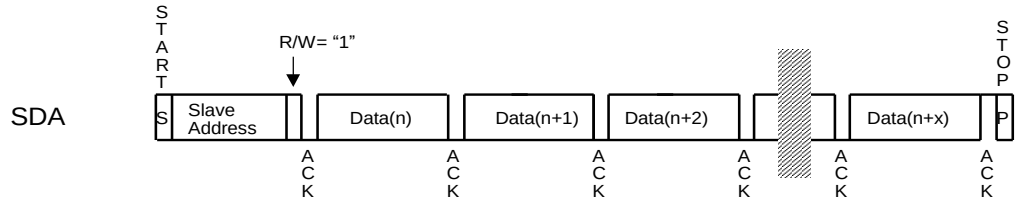


Figure 25. Current Address Read

(2)-2 Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4499EX then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4499EX ceases the transmission.

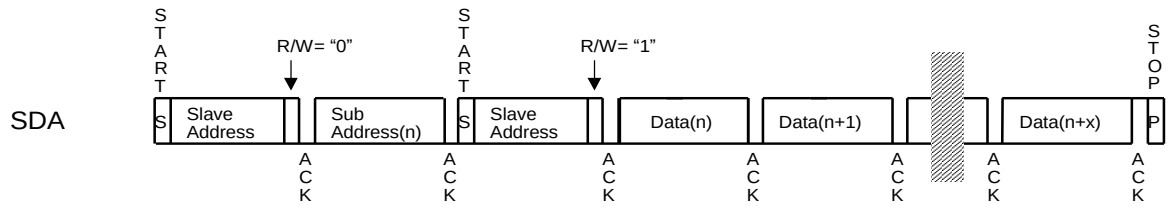


Figure 26. Random Address Read

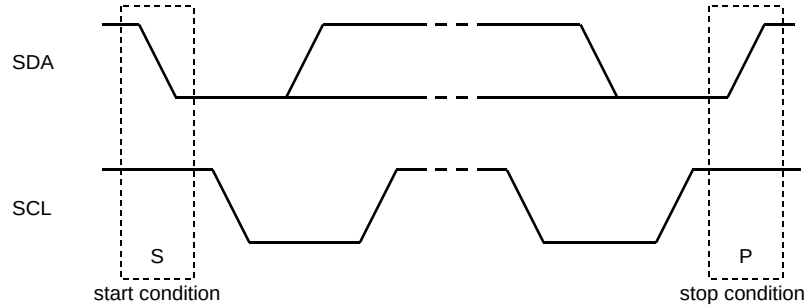


Figure 27. Start Condition and Stop Condition

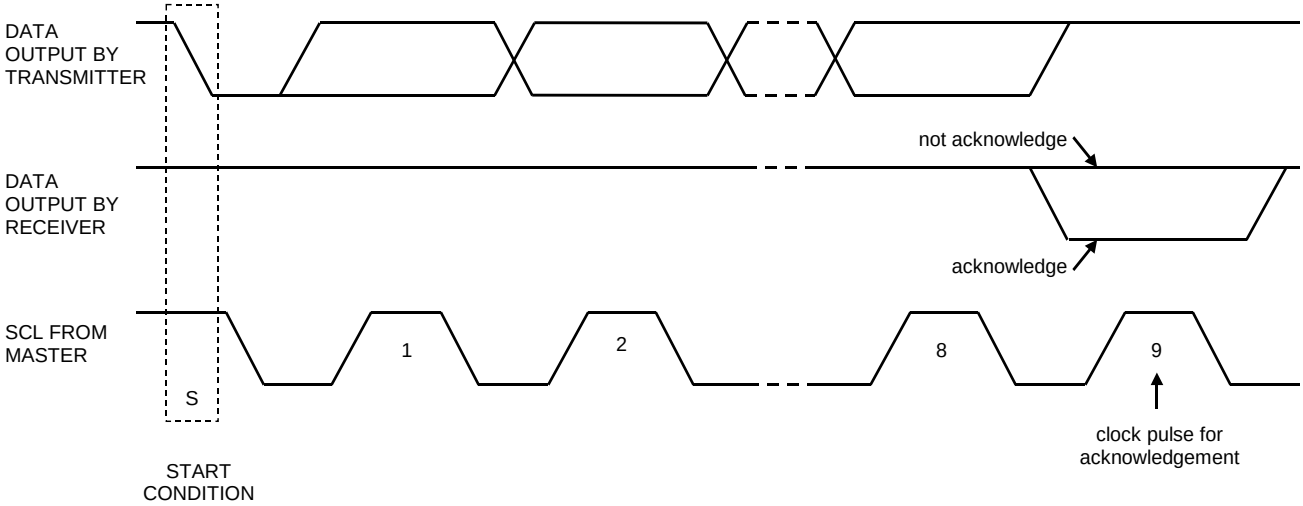


Figure 28. Acknowledge (I^2C-Bus)

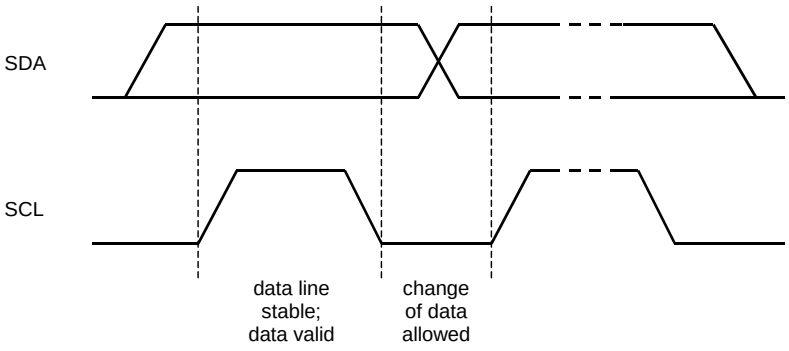


Figure 29. Bit Transfer (I^2C-Bus)

9.11. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00H	Control1	MSTBN	VTSEL	OSR	STME	LSELN	RSELN	STBY	MUTEN	00
01H	Control2	SC	DSEL[4]	0	0	0	0	INVL	INVR	00
02H	Control3	DSEL[3]	DSEL[2]	DSEL[1]	DSEL[0]	0	0	0	TST	00

Notes:

(1) In 3-wire serial control mode, the AK4499EX does not support read commands.
(2) The AK4499EX supports read command in I^2C-Bus control mode.
(3) If the address exceeds “02H”, the address counter will “roll over” to “00H” and the next write/read address will be “00H”.
(4) Bits indicated as 0 in each address must contain a “0” value. Malfunctions may occur if writing “1” value to these bits.
(5) Writing after 03H is forbidden. Malfunctions may also occur by this action.
(6) When the PDN pin goes to “L”, the registers are initialized to their default values.

9.12. Register Definitions

【00H】

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control1	MSTBN	VTSEL	OSR	STME	LSELN	RSELN	STBY	MUTEN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MUTEN: The AK4499EX is set in Mute state (Table 10).
0: Mute (default)
1: Normal Operation

STBY: Standby ON/OFF control bit
0: Normal Operation (default)
1: Standby

LSELN, RSELN:
Input and output combination can be changed by LSELN bit and RSELN bit (Table 6).

STME: Audio interface format mode select bit (Table 5).
0: Multi-bit Mono mode (default)
1: Multi-bit Stereo mode

OSR: Sampling speed mode setting bit (Table 3).
0: OSR256 mode (default)
1: OSR128 mode

VTSEL: Digital input voltage level of MCLK select bit.
0: High Level = 1.36 V, Low Level = 0.34 V (default)
1: High Level = 2.2 V, Low Level = 0.8 V

MSTBN: Stand-by mode by MCLK input enable.
0: enable (default)
1: disable

【01H】

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control2	SC	DSEL [4]	0	0	0	0	INVL	INVR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INVL, INVR:
The output signal phase can be inverted by INVL bit and INVR bit (Table 8).

DSEL [4]: “0” value must be written to this bit. Otherwise, malfunction may occur.

SC: Sound control
0: Measurement mode (default)
1: Sound quality mode

【02H】

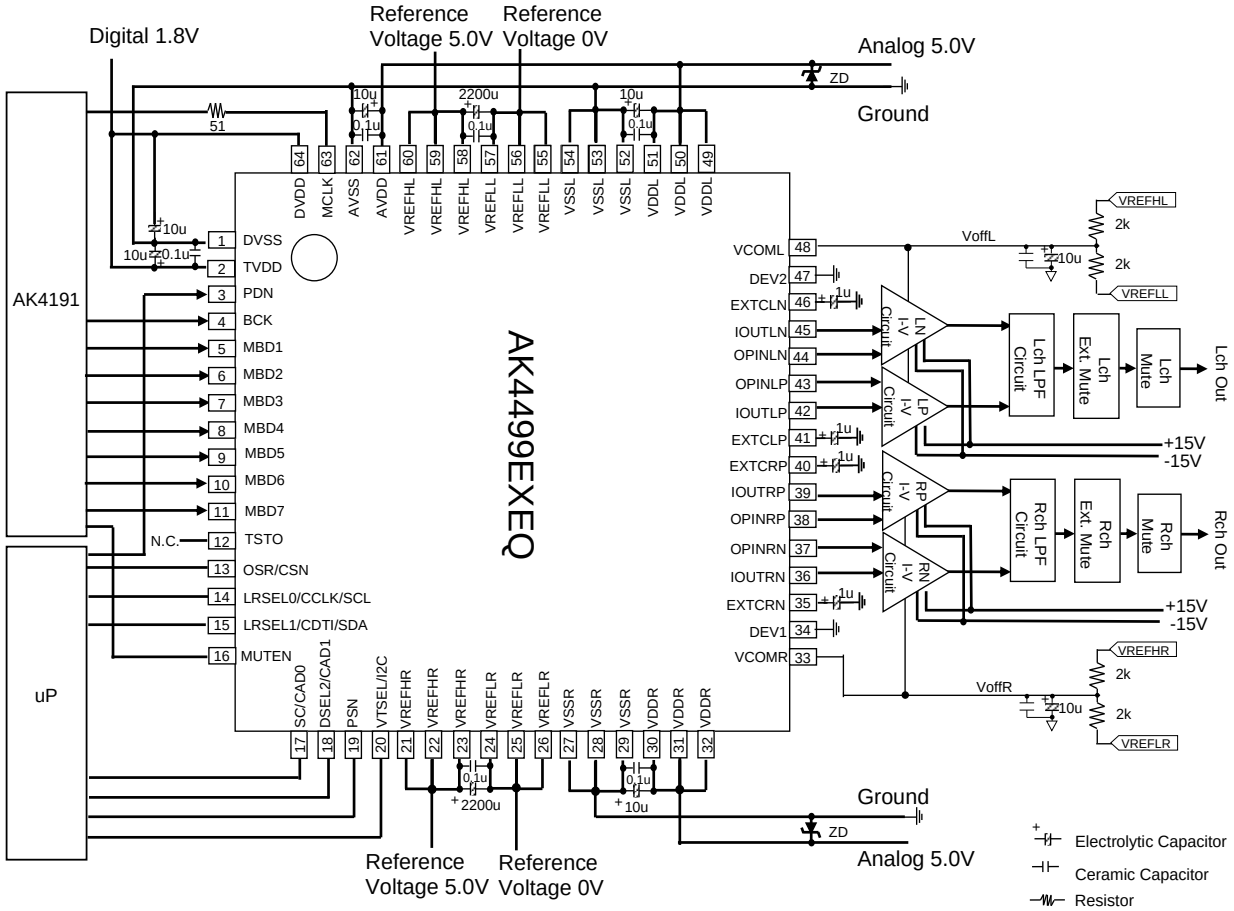
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control3	DSEL [3]	DSEL[2]	DSEL[1]	DSEL[0]	0	0	0	TST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

TST: Test bit. “0” value must be written to this bit. Otherwise, malfunction may occur.

DSEL [3:0]: “0100” value must be written to this bit. Otherwise, malfunction may occur.

10. Recommended External Circuits

10.1. External Connection Example



(AVDD = VDDL/R = VREFHL/R = 5.0 V, TVDD = DVDD = 1.8V, Register Control Mode)

Notes:

(1) Power lines of AVDD, TVDD and VDDL/R should be distributed separately, from the point with low impedance of regulators or other parts.

(2) AVSS, DVSS add VSSL/R must be connected to the same ground. (The ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)

(3) Connect VCOML/R and positive input pin of I-V conversion op-amp from the midpoint each Voff circuits that connects VREFHL/R and VREFLL/R via the external voltage divider resistors. Voff lines do not connect any other pins except VCOML/R and positive input pins.

(4) It is recommended to input MCLK via a 51 Ω damping resistor. Without the resistor, there is a possibility that THD+N characteristic degrades because of high-frequency noise of MCLK.

(5) All digital input pins except pull-up pins should not be allowed to float.

(6) There is a possibility of IC destruction due to breakdown of the withstanding voltage of the analog output pins (IOUTLP/LN/RP/RN). Connect a Zener diode (V_{RWM} = 6 to 7 V) between each VDDL/R and VSSL/R if the power up/down sequence shown in Figure 13 cannot be followed.

(7) Figure 35 is not necessary for the AK4499EX. Refer to 10.5. External Mute Circuit for details.

Figure 30. Typical Connection Diagram

10.2. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD and VDDL/R. AVDD and VDDL/R are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL/R should be distributed separately, from the point with low impedance of regulators or other parts.

AVSS, DVSS and VSSL/R must be connected to the same ground. Decoupling capacitors for high frequency should be placed as near as possible to the AK4499EX.

10.3. Reference Voltage

The differential voltage between the VREFHL/R pins and the VREFLL/R pins set the analog output current. The VREFHL/R pins are normally connected to 5.0V reference voltage, and the VREFLL/R pins are normally connected to the 0V reference voltage. Connect a 0.1 μF ceramic capacitor and 2200 μF electrolytic capacitor between the VREFHL/R pins and the VREFLL/R pins.

The VREFHL/R and VREFLL/R pins should avoid noises from other power supplies. Connect the VREFHL/R to the analog 5.0V via a 1 Ω resistor, and the VREFLL/R pins to the analog ground via a 1 Ω resistor when it is difficult to obtain expected analog characteristics because of noises from other power supplies (A low pass filter of fc = 36 Hz will be composed with the 2200 μF capacitor and the 1 Ω resistor. It removes signal frequency noise from other power supply lines). However, the direct voltage at the VREFHL/R and VREFLL/R pins drops ±23 mV since a current of ±23 mA flows at VREFH/L via 1 Ω resistor.

The ceramic capacitors should be connected as near as possible to the pins. All digital signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins to avoid unwanted coupling into the AK4499EX.

10.4. Analog Output

Figure 31 shows an example of Lch external I-V conversion circuit of the AK4499EX. The analog outputs are full differential current outputs. The Differential Output Current (IOUTP - IOUTN) is 72.8 mApp (typ.). The output current is converted to voltage by the I-V conversion circuit. The common voltage of the current output pins (IOUTLN/LP/RN/RP, OPINLN/LP/RN/RP) is 2.5 V(typ.). The common voltage of the signal after I-V conversion (VOUTLP/LN/RP/RN) can be adjusted by changing the positive inputs of op-amp for I-V conversion and the VCOML/R input from (VREFHL/L + VREFLL/R)/2. For example, input Voff = 1.9 V to obtain 0 V signal common voltage at Rfb = 360 Ω.

The output range of I-V conversion is 4.6 Vrms centered around signal common voltage, and 9.2 Vrms after differential summing. IOUTLP/RP current and IOUTLN/RN current cannot be summed. The differential outputs are summed externally after I-V conversion.

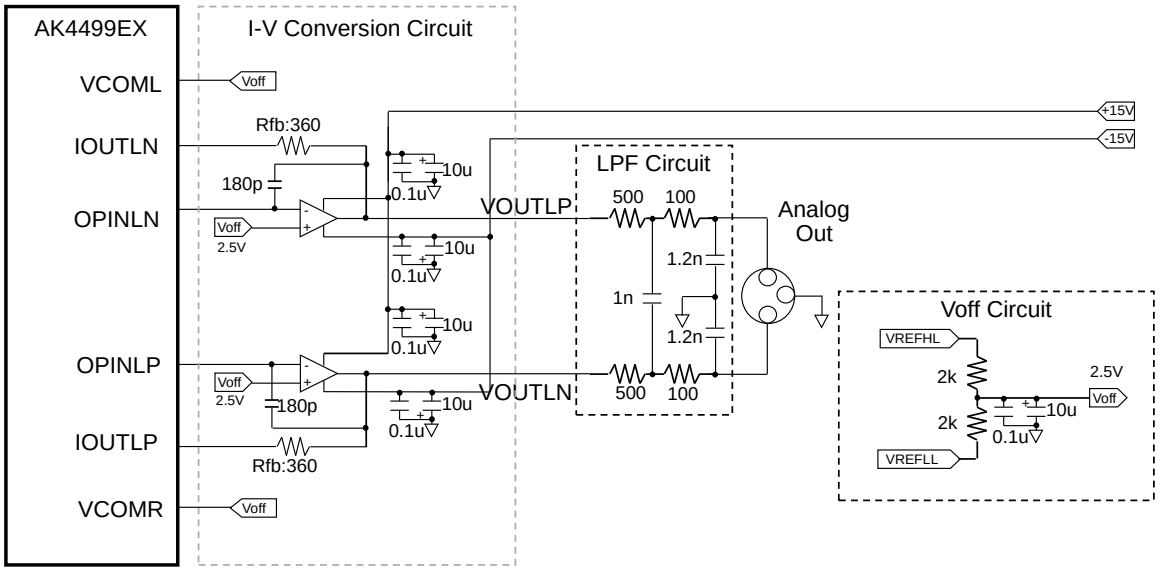


Figure 31. Lch External I-V Conversion Circuit Example (same for Rch)

Notes:

(1) Input voltage range of the positive input of op-amp for I-V conversion circuit is from 0.5 V (typ.) to 2.5 V (typ.). The signal common voltage (VOUTLP and VOUTLN) does not have to be 0 V.

(2) Resistors used in the I-V conversion circuit are recommended to be within 0.1 % of absolute error to meet specifications.

Table 13. Frequency Response of Differential Output Circuit

Gain (1 kHz, typ.)		0.0 dB
Frequency Response (ref: 1 kHz, typ.)	20 kHz	-0.18 dB
	40 kHz	-0.69 dB
	80 kHz	-2.28 dB

10.4.1. Mono mode

In mono mode, connect I-V conversion voltage output terminals with resistors and take differential output from the midpoint (Voff) of the connection as shown in Figure 32.

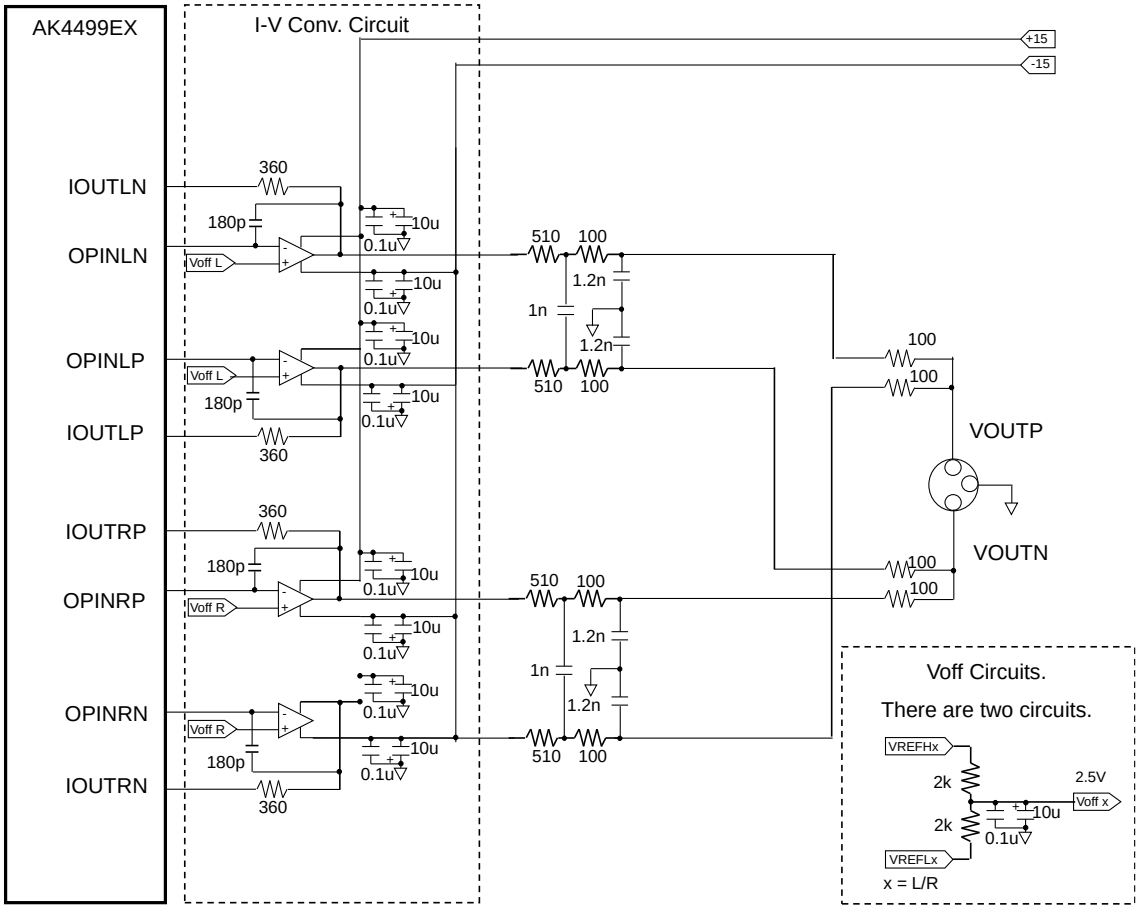


Figure 32. External I-V Conversion Circuit Example (Mono mode)

10.4.2. External Analog Low Pass Filter Example

Differential voltage signal after I-V conversion is summed by differential summing circuit (low pass filter). Figure 33 shows an example of differential summing circuit and Table 14 shows the frequency response.

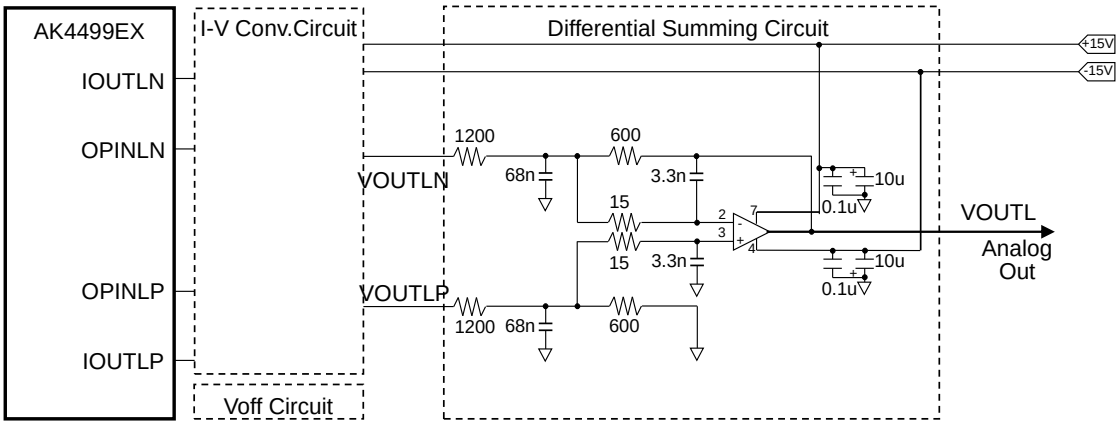


Figure 33. External 2nd Order LPF Circuit Example for PCM mode (fc = 112 kHz (typ.), Q = 0.692 (typ.))

Table 14. Frequency Response of External LPF Circuit Example

Gain (1 kHz, typ.)		-6.02 dB
Frequency Response (ref:1 kHz, typ.)	20 kHz	-6.04 dB
	40 kHz	-6.14 dB
	80 kHz	-7.19 dB

10.4.3. Feedback Loop of External Operational Amplifier

Figure 34 shows the internal state of the AK4499EX when the analog output is Hi-Z and when the analog output is “0” data output. Feedback loop of the external amplifier is always maintained while the power supply of the AK4499EX is on.

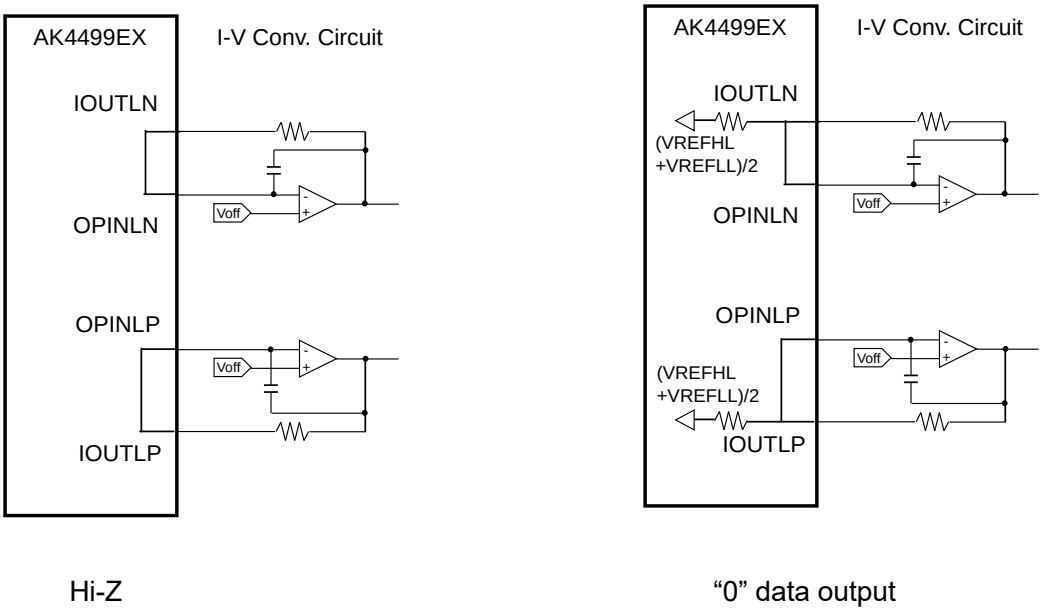


Figure 34. Internal State of the AK4499EX when Outputting Hi-Z or “0” data output

10.5. External Mute Circuit

Click noise may occur due to DC offset if the power up/down sequence shown in Figure 13 cannot be followed and external operational amplifier is powered up before the AK4499EX. Connect external mute circuits shown in Figure 35 to analog signal lines to prevent a click noise. The external mute circuit should be connected to the signal after I-V conversion (Figure 30). Base current will be input to the transistor RN2202 when the power (5.0 V typ.) is not supplied to the VDDL/R pins. In this case, emitter current flows to the 2SC3327 via 3.8 kΩ resistance as base current and the analog signal line is short to the signal ground. Note that there is a possibility that THD+N performance degrades about 3 dB by connecting an external mute circuit.

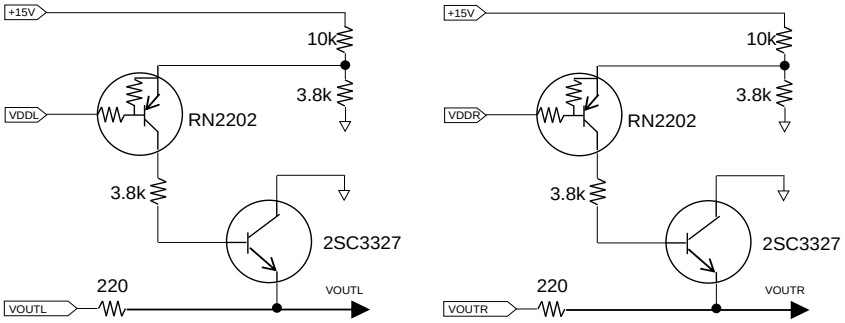
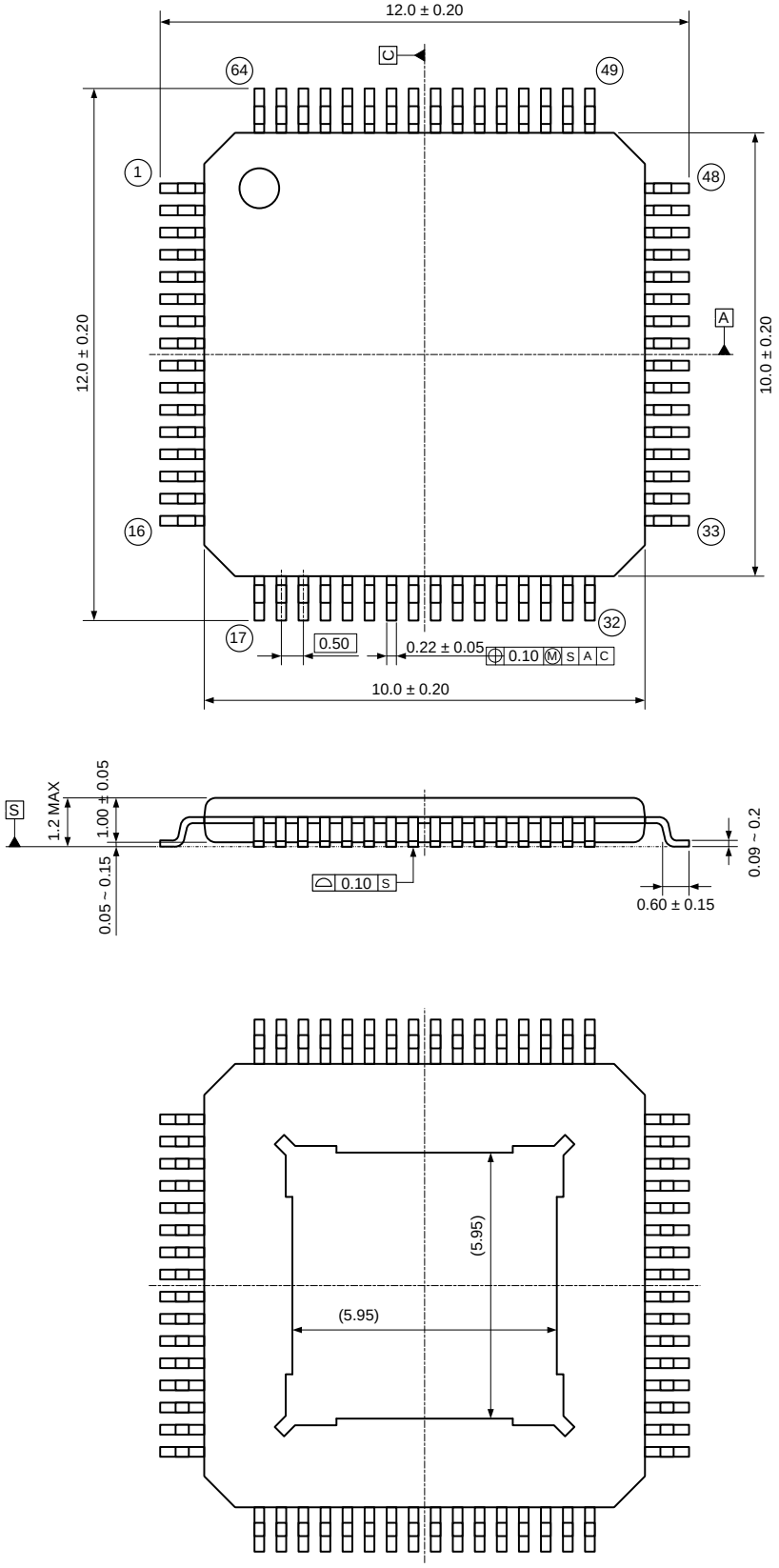


Figure 35. External Mute Circuit Example

11. Package

11.1. Outline Dimensions

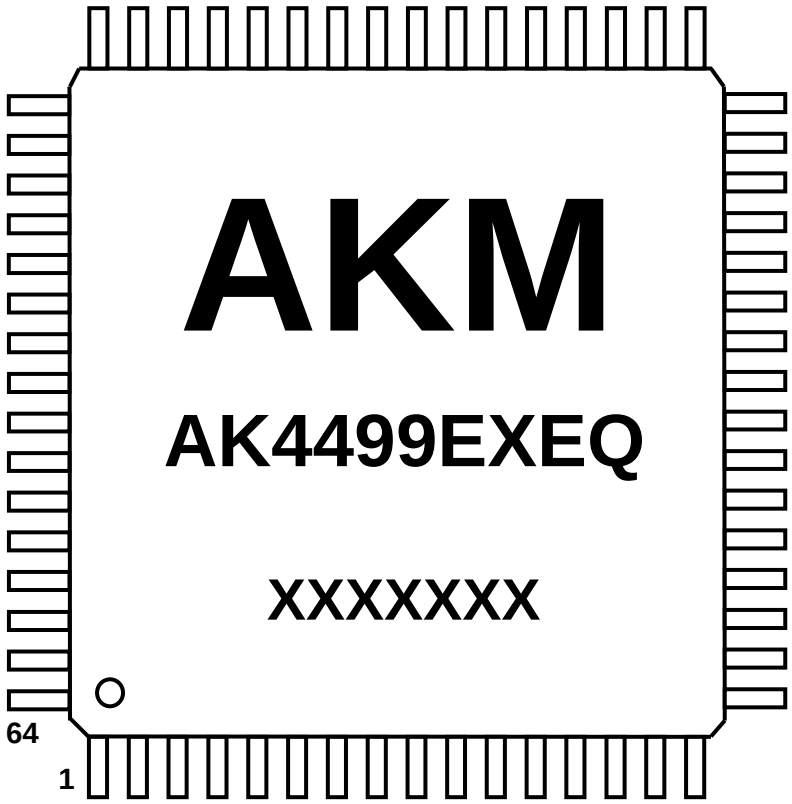
64-pin HTQFP10×10 (Unit: mm)



11.2. Material & Terminal Finish

Package molding compound:	Epoxy, Halogen (Br and Cl) free
Lead frame material:	EFTEC-64T
Terminal surface treatment:	Solder (Pb free) plate

11.3. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4499EXEQ
4) AKM Logo

12. Ordering Guide

AK4499EXEQ	-40 to +85 °C	64-pin HTQFP (0.5 mm pitch)
AKD4499EX	Evaluation Board for AK4499EX	

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
22/07/dd	00	First Edition		

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