AK4191 and AK4499EX
Application Note

1. General Description

This application note is intended to assist in designing systems using the AK4191 and the AK4499EX.

2. Table of Contents

3. Acronyms

	Description
PCM	Pulse Code Modulation
DSD	Direct Stream Digital
FS	Sampling Frequency
FSB	Base Sampling Frequency (ex. FSB is 48 kHz when FS = 48, 96,192, 384, 768 or 1536 kHz.) (ex. FSB is 44.1 kHz when FS = 44.1, 88.2,176.4, 352.8, 705.6 or 1411.2 kHz.)
FCK	Frequency of MCLK
FCKB	Base Frequency of MCLK. FCKB is calculated by the formula 256 * FSB.
OSR	Over Sampling Ratio
X'tal	Crystal Oscillator
PLL	Phase Locked Loop
MCU	Micro Controller Unit
FIFO	First In First Out
FPGA	Field Programmable Gate Array
DSP	Digital Signal Processor

4. Basic Instructions to be Observed

4.1. Device Connection Example and Basic Instructions to be Observed

Figure 1 shows connection example when using the AK4191 and AK4499EX as a set. There are four basic instructions that must be observed.

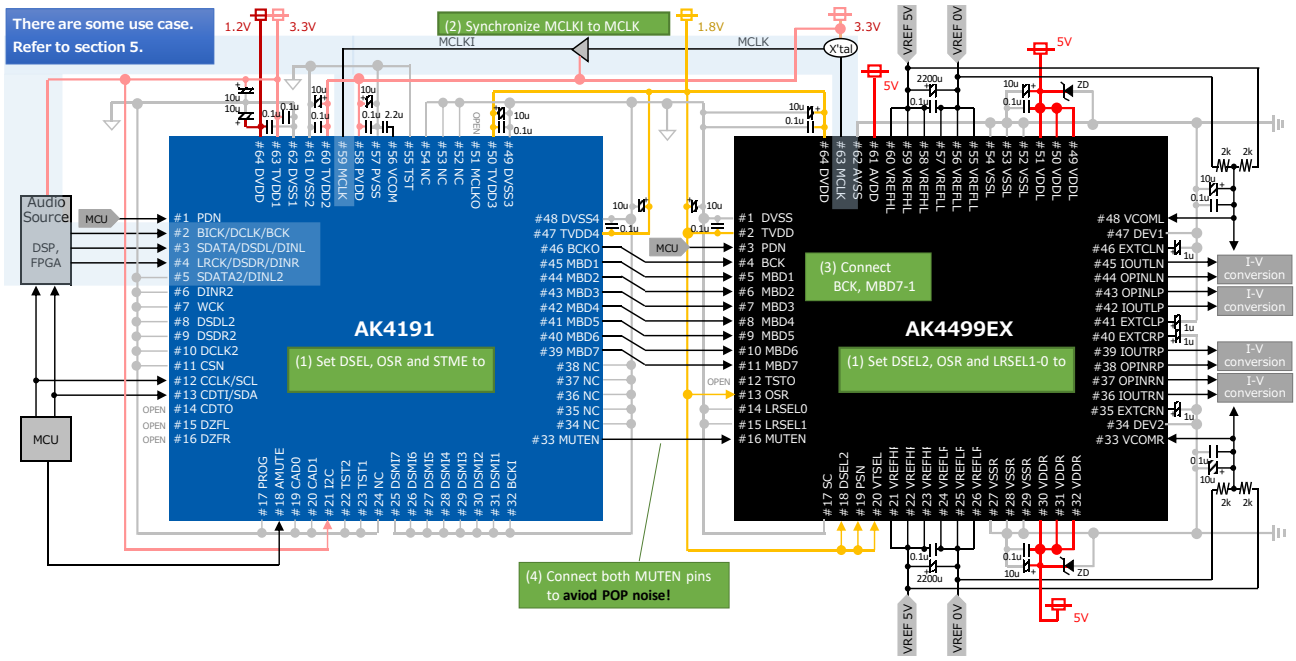


Figure 1. Connection example of the AK4191 and the AK4499EX

(1) The settings shown in Table 1 must correspond to those of AK4191 and AK4499EX. “DSEL” must be set to specified value. BCK frequency is selected by setting OSR bit of the AK4191 and MBD7-1 data format is selected by setting OSTME bit of the AK4191. OSR pin and LRSEL1-0 pins of the AK4499EX (OSR bit and STME bit when the AK4499EX is in Register control mode) must be set to correspond to the AK4191 settings.

--- Refer to the following three sections of the AK4191 datasheet.
--- 9.2.2. BCKO
--- 9.3.4. MBD1-7 Output Format
--- Refer to following section in the AK4499EX datasheet.
--- 9.2. System Clock

Table 1. Settings to be corresponded

	AK4191		AK4499EX			
	-		Pin Control mode		Register Control Mode	
	Register name	Setting	Pin name	Setting	Register name	Setting
Device Setting	DSEL[7:0]	“21H”	DSEL2	“H”	DSEL[3:0]	“0100”
BCK frequency	OSR	128fs or 256fs	OSR	Same as the AK4191	OSR	Same as the AK4191
MBD7-1 data format	OSTME	Stereo or Mono	LRSEL1-0 pins	Same as the AK4191	STME	Same as the AK4191

(2) The frequency of MCLKI input to the AK4191 and MCLK input to the AK4499EX can be different, but they must be synchronized.

--- Refer to following section in the AK4191 datasheet.
--- 9.1.3.1. Asynchronous and Synchronous Modes

(3) #46 BCKO pin of the AK4191 must be connected to #4 BCK pin of the AK4499EX and each #39-45 MBD7-1 pins of the AK4191 must be connected to each #11-5 MBD7-1 pins of the AK4499EX. The analog characteristics of the AK4499EX are specified when the AK4191 is used with DSMSEL[1:0] bits “00” and OBIT[1:0] bits “00”.

--- Refer to following section in the AK4499EX datasheet.
--- 8.1. Analog Characteristics

(4) It is recommended to connect #33 MUTEN pin of the AK4191 and #16 MUTEN pin of the AK4499EX. In this way, the AK4191 can control the AK4499EX and avoid noise that occurs when switching audio sources. Also, if a flag indicating an abnormal state such as the PLL unlock flag of the Audio Source Device to #18 AMUTE pin of the AK4191, it can directly control the AK4499EX and set MUTE state in abnormal conditions. This function can be used whether the AK4499EX is in Pin Control mode or Register Control mode.

--- Refer to 6. POP noise free solution in this document.

(5) The AK4499EX executes the initialize sequence after changing #16 MUTEN pin (or MUTEN bit) of the AK4499EX from “L” to “H”. To do this sequence correctly, the MCLK frequency, BCK frequency, and OSR pin (or OSR bit) settings for the AK4499EX should be changed while #16 MUTEN pin is "L", and MUTEN should be set to "H" after the MCLK and BCK frequencies are stable. It is recommended to refer to the sequence diagrams in the following sections of this document, which are appropriate for your use case.

--- 5.1.2. Audio Source Switching Sequence (Case1)
--- 5.2.2. Audio Source Switching Sequence (Case2)
--- 5.3.2. Audio Source Switching Sequence (Case3)

Also, it is recommended to refer 6. POP noise free solution in this document, which describes the conditions under which MUTEN becomes “L”.

4.2. Register setting example

These are the register settings example of the AK4191 when used in the connection example in Figure 1. Set "1" to the registers colored red. The registers colored blue should be set to "1" during audio signal playback and "0" depending on the situation.

Table 2. AK4191 Register map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	DUAL	EXDF	MUTES[1]	MUTES[0]	DIF[2]	DIF[1]	DIF[0]	RSTN
01H	Control 2	0	0	SSLOW	SD	SLOW	DEM[1]	DEM[0]	SMUTE
02H	Control 3	DP	ADP	0	DCKB	DDMOE	DZFE	DZFM	DZFB
03H	Lch ATT	ATTL[7]	ATTL[6]	ATTL[5]	ATTL[4]	ATTL[3]	ATTL[2]	ATTL[1]	ATTL[0]
04H	Rch ATT	ATTR[7]	ATTR[6]	ATTR[5]	ATTR[4]	ATTR[3]	ATTR[2]	ATTR[1]	ATTR[0]
05H	Control 4	INVL	INVR	SELLR	MONO	DFS[2]	DFS[1]	DFS[0]	MSN
06H	DSD1	DDM	DML	DMR	DDMT	DSDD	DSDSEL [2]	DSDSEL [1]	DSDSEL [0]
07H	Control 5	ATS[1]	ATS[0]	0	GC[3]	GC[2]	GC[1]	GC[0]	SYNCE
08H	Control 6	BCKS[1]	BCKS[0]	MCKOE	MCKDV	MCKS[1]	MCKS[0]	FS32K	PMPLL
09H	DSD2	0	0	0	0	0	0	DSDF	DSDPATH
0AH	Control 7	TDM[1]	TDM[0]	SDS[2]	SDS[1]	SDS[0]	0	OSTME	ISTME
0BH	Control 8	0	0	0	0	0	0	0	DSYNCE
0CH	DSMI/O	DSMIFS	MBDZ	DSMSEL [1]	DSMSEL [0]	0	OBIT[1]	OBIT[0]	OSR
0DH	DSMI	ATSMX [1]	ATSMX [0]	GAIN2L	GAIN2R	IBIT	SUBL	SUBR	PMDSMI
0EH	FB ATTL	ATTMXL [7]	ATTMXL [6]	ATTMXL [5]	ATTMXL [4]	ATTMXL [3]	ATTMXL [2]	ATTMXL [1]	ATTMXL [0]
0FH	FB ATTR	ATTMXR [7]	ATTMXR [6]	ATTMXR [5]	ATTMXR [4]	ATTMXR [3]	ATTMXR [2]	ATTMXR [1]	ATTMXR [0]
10H	Reserved	DSEL[7]	DSEL[6]	DSEL[5]	DSEL[4]	DSEL[3]	DSEL[2]	DSEL[1]	DSEL[0]
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Control 9	ADPE	ADPT[1]	ADPT[0]	0	0	ADFS[2]	ADFS[1]	ADFS[0]
16H	Control 10	0	0	0	0	ADCKS	ADSDS[2]	ADSDS[1]	ADSDS[0]

Table 3. AK4191 Settings details

Function	Register name	Setting
Automatic Data Conversion Mode (PCM / DSD) Switching	ADPE, DDM	Enable
DSD data input pin select	DSDPATH	#2, #3, #4 pins
MCLK Input Frequency	MCKS[1:0]	22.5792 MHz
DSD Auto Sampling Speed Mode Setting	ADCKS	Enable
PCM Audio Interface Format	DIF[2:0]	32-bit MSB justified
Gain Adjustment Function	GC[3:0]	80% (same as the AK4499EQ)
Digital Attenuator	ATTL[6:0], ATTR[6:0]	0dBFS
Delta Sigma Modulator Data zero output	MBDZ	Enable
BCKO Frequency	OSR	5.6448 MHz
Delta Sigma Modulator Data Output (MBD7-1) Format	OSTME	Stereo

5. Clock and Audio Input Signal Connections

There are three main use cases, depending on whether MCLK is distributed from AK4499EX side or the Audio Input side and whether or not MCLK is synchronized to the Input Signal of the AK4191.

Table 4. Clock synchronization use cases

	Input Signal of the AK4191 is synchronized to MCLK or not.	Where to distribute MCLK from	
Case1	Not synchronized	AK4499EX Side	Refer to 5.1
Case2	Synchronized	AK4499EX Side	Refer to 5.2
Case3	Synchronized	Audio Input Side	Refer to 5.3

5.1. Input Signal of AK4191 is not synchronized to MCLK distributed from AK4499EX side.

This use case features **a low-jitter D/A conversion solution without complex control**. The AK4499EX can use a low-jitter clock such as a crystal oscillator regardless of the synchronization relationship between audio input signal and MCLK, thus enabling high-precision signal reproduction.

5.1.1. Connection example

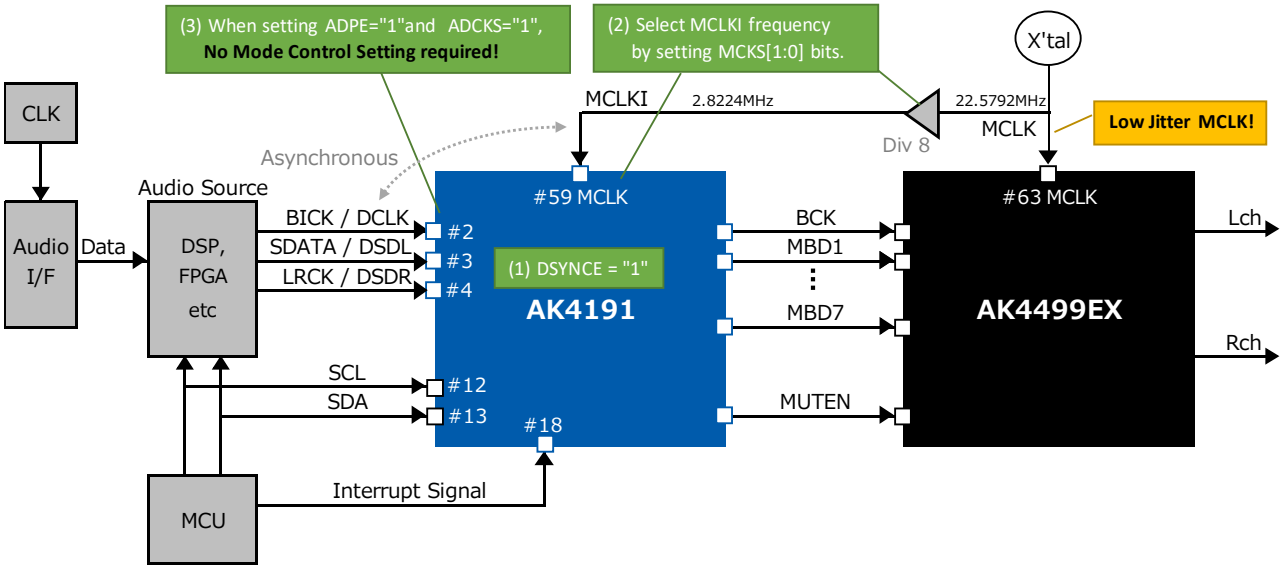


Figure 2. Connection example when using AK4191 in asynchronous mode

Notes:

(1) In this use case, the AK4191 should be set Asynchronous mode by setting DSYNCE bit = ”1”. The sampling frequency of audio input signal and MCLK frequency are supported only at rates of 44.1 kHz * 2^N or 48 kHz * 2^N.

--- Refer to following section in the AK4191 datasheet.
--- 9.1.3.1. Asynchronous and Synchronous Modes

(2) This example uses a frequency divider to avoid long wiring for transmitting high frequency clock, but it can be changed to a clock buffer. MCKS[1:0] bits of the AK4191 should be set corresponding to the frequency of MCLKI. In this example they should be set “10”.

--- Refer to following section in the AK4191 datasheet.

--- 9.2.1.1. MCLK input

(3) When setting ADPE bit = “1” and ADCKS = “1”, the AK4191 automatically sets the optimal data conversion mode such as PCM mode or DSD mode and sampling speed mode internally. No data conversion mode or sampling speed mode settings are required, but switching operation should be done while RSTN bit of the AK4191 is set “0”. Thus the AK4191 will generate MUTEN output signal to avoid noise that occurs when switching audio sources.

--- Refer to the following sections in this document.
--- 5.1.2. Audio Source Switching Sequence
--- 6. POP noise free solution
--- Refer to the following sections of the AK4191 datasheet.
--- 9.2.3.1. Slave Mode (MSN bit = ”0”)
--- 9.2.4.2. Auto Setting Mode (ADCKS bit = ”1”)
--- 9.10. Automatic Data Conversion Mode Switching

5.1.2. Audio Source Switching Sequence

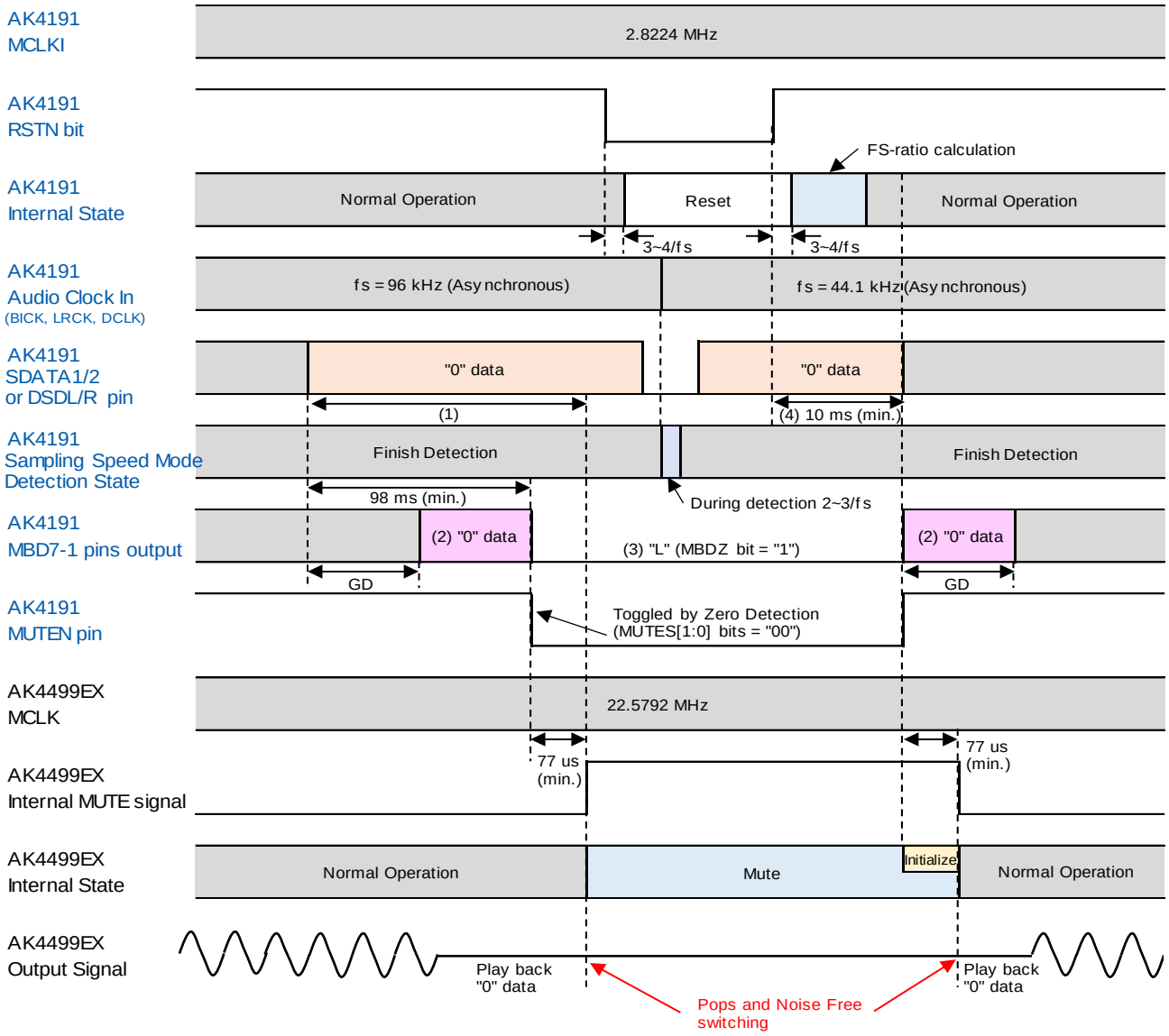


Figure 3. Clicks and Pops free switching sequence example using AK4191 in asynchronous mode

Notes:

(1) It is recommended that data zero input in AK4191 is held until internal MUTE signal of AK4499EX goes to “L” to avoid Clicks and Pops during mode switching (min. 4096 * 256 / FCKB + 77 [us]).

(2) MBD7-1 outputs Delta-Sigma’s zero data with out-of-band noise.

(3) The AK4191 has Delta Sigma Modulator Data zero output function. This function is enabled by setting MBDZ bit = ”1”. MBD1-7 pins go to “L” when MUTEN pin outputs “L”.

(4) It is recommended to hold input data zero for more than 10 ms until a sampling ratio calculaton for data synchronization is finished after setting RSTN bit = ”1”.

5.2. Input Signal of the AK4191 is synchronized to MCLK distributed from AK4499EX side.

This use case features **a low-jitter D/A conversion solution with switching MCLK**. The AK4499EX can use a low-jitter clock such as a crystal oscillator by selecting synchronized frequency clocks, thus enabling high-precision signal reproduction. In this use case, the AK4191 should be set Synchronous mode by setting DSYNCE bit = ”0”.

5.2.1. Connection example

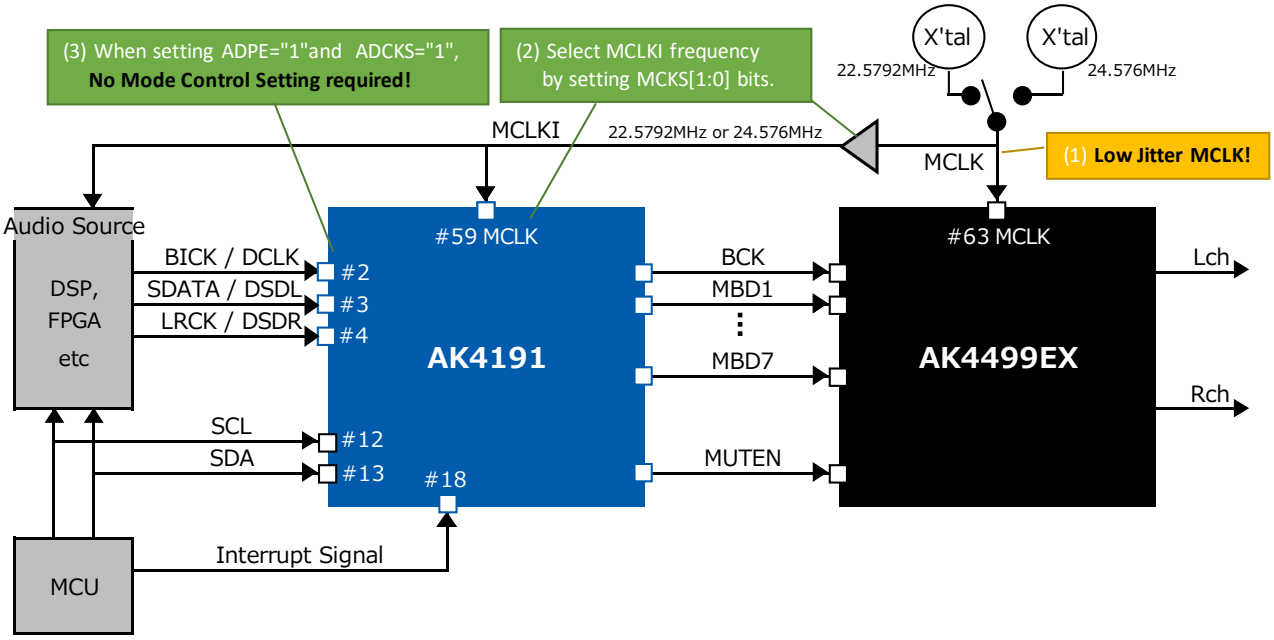


Figure 4. Connection example when using AK4191 in synchronous mode

Notes:

(1) MCLK frequency should be switched to the frequency corresponding to FSB while PMPLL bit of the AK4191 is "0". When PMPLL bit is set “0”, MUTEN signal goes to “L” immediately and the AK4499EX goes to MUTE state. So there is no need to control the AK4499EX.

--- Refer to following section in the AK4191 datasheet.
--- 9.2.1.1. MCLK input
--- Refer to following section in the AK4499EX datasheet.
--- 9.9. Internal State

(2) This example uses a clock buffer, but it can be changed to a frequency divider to avoid long wiring for transmitting high frequency clock. MCKS[1:0] bits of the AK4191 should be set corresponding to the frequency of MCLKI. In this example they should be set “01”.

--- Refer to following section in the AK4191 datasheet.
--- 9.2.1.1. MCLK input

(3) When setting ADPE bit = “1” and ADCKS = “1”, the AK4191 automatically sets the optimal data conversion mode such as PCM mode or DSD mode and sampling speed mode internally. No data conversion mode or sampling speed mode settings are required. If audio sources are switched with zero data, the AK4191 will generate MUTEN output signal to avoid noise.

--- Refer to the following sections in this document.
--- 5.2.2. Audio Source Switching Sequence

--- 6. POP noise free solution

--- Refer to the following sections of the AK4191 datasheet.

--- 9.2.3.1. Slave Mode (MSN bit = ”0”)

--- 9.2.4.2. Auto Setting Mode (ADCKS bit = ”1”)

--- 9.10. Automatic Data Conversion Mode Switching

5.2.2. Audio Source Switching Sequence

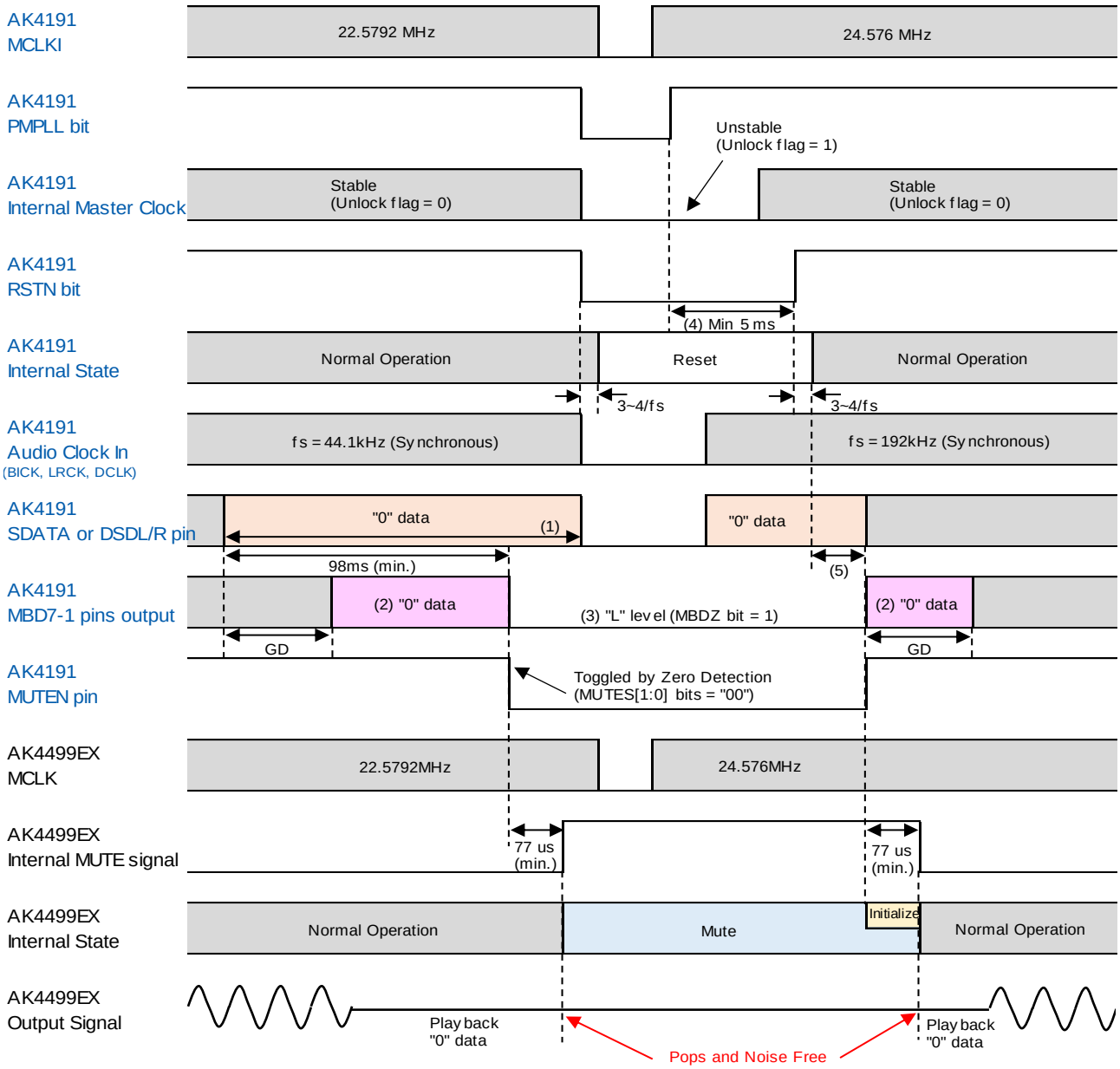


Figure 5. Clicks and Pops free switching sequence example using AK4191 in synchronous mode

Notes:

(1) It is recommended that data zero input in AK4191 is held until internal MUTE signal of AK4499EX goes to “L” to avoid Clicks and Pops during mode switching (min. 4096 * 256 / FCKB + 77 [us]).

(2) MBD7-1 outputs Delta-Sigma’s zero data with out-of-band noise.

(3) The AK4191 has Delta Sigma Modulator Data zero output function. This function is enabled by setting MBDZ bit = ”1”. MBD1-7 pins go to “L” when MUTEN pin outputs “L”.

(4) RSTN bit should be set to “1” with an interval of 5 ms (min.) for stabilization of PLL circuit after clock reset is released.

(5) It is recommended that data zero input in AK4191 is held 77 us (min.) after Internal reset state of AK4191 is released.

5.3. Input Signal of the AK4191 is synchronized to MCLK distributed from the Audio Input side.

This use case features **a simple D/A conversion solution**. In this case, there is one clock source which is synchronized to audio input. In this use case, the AK4191 should be set Synchronous mode by setting DSYNCE bit = ”0”.

5.3.1. Connection example

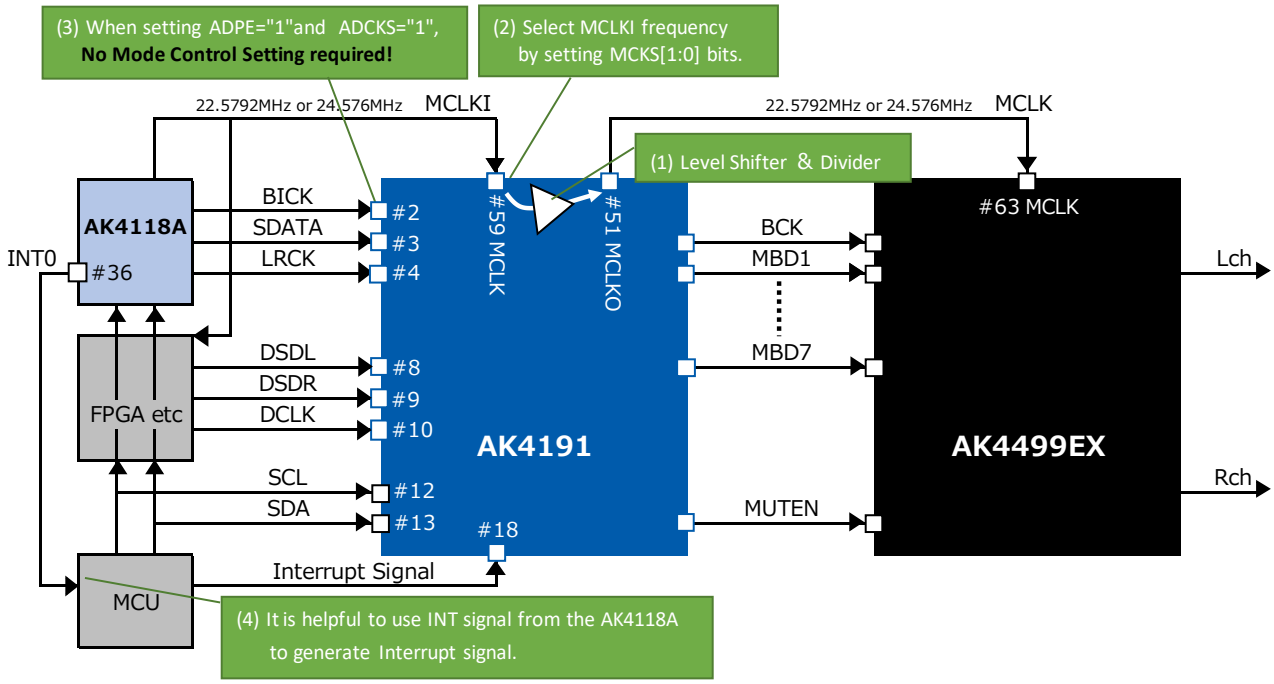


Figure 6. Connection example when using AK4191 in synchronous mode with DIR

Notes:

(1) The AK4191 has a level shifter and a frequency divider between MCLKI input via pin #59 and MCLKO output via pin #51. Power supply TVDD2, mainly for MCLKI input, and power supply TVDD3, mainly for MCLKO output, are independent of each other and isolated from other power supplies.
MCLKI frequency should be switched while PMPLL bit of the AK4191 is "0". When PMPLL bit is set “0”, MUTEN signal goes to “L” immediately and the AK4499EX goes to MUTE state. So there is no need to control the AK4499EX.

--- Refer to following section in the AK4191 datasheet.
--- 9.2.1.1. MCLK input
--- Refer to following section in the AK4499EX datasheet.
--- 9.9. Internal State

(2) MCKS[1:0] bits of the AK4191 should be set corresponding to the frequency of MCLKI. In this example they should be set “01”.

--- Refer to following section in the AK4191 datasheet.
--- 9.2.1.1. MCLK input

(3) When setting ADPE bit = “1” and ADCKS = “1”, the AK4191 automatically sets the optimal data conversion mode such as PCM mode or DSD mode and sampling speed mode internally. No data

conversion mode or sampling speed mode settings are required. If audio sources are switched with zero data, the AK4191 will generate MUTEN output signal to avoid noise.

--- Refer to the following sections in this document.
--- 5.3.2. Audio Source Switching Sequence
--- 6. POP noise free solution
--- Refer to the following sections of the AK4191 datasheet.
--- 9.2.3.1. Slave Mode (MSN bit = ”0”)
--- 9.2.4.2. Auto Setting Mode (ADCKS bit = ”1”)
--- 9.10. Automatic Data Conversion Mode Switching

(4) It is helpful to use INT0 output via #36 INT0 of the AK4118A to generate interrupt signal. Thus, the AK4191 can directly control the AK4499EX and set MUTE state in abnormal conditions. This function can be used whether the AK4499EX is in Pin Control mode or Register Control mode.

--- Refer to the following sections in this document.
--- 6. POP noise free solution

5.3.2. Audio Source Switching Sequence

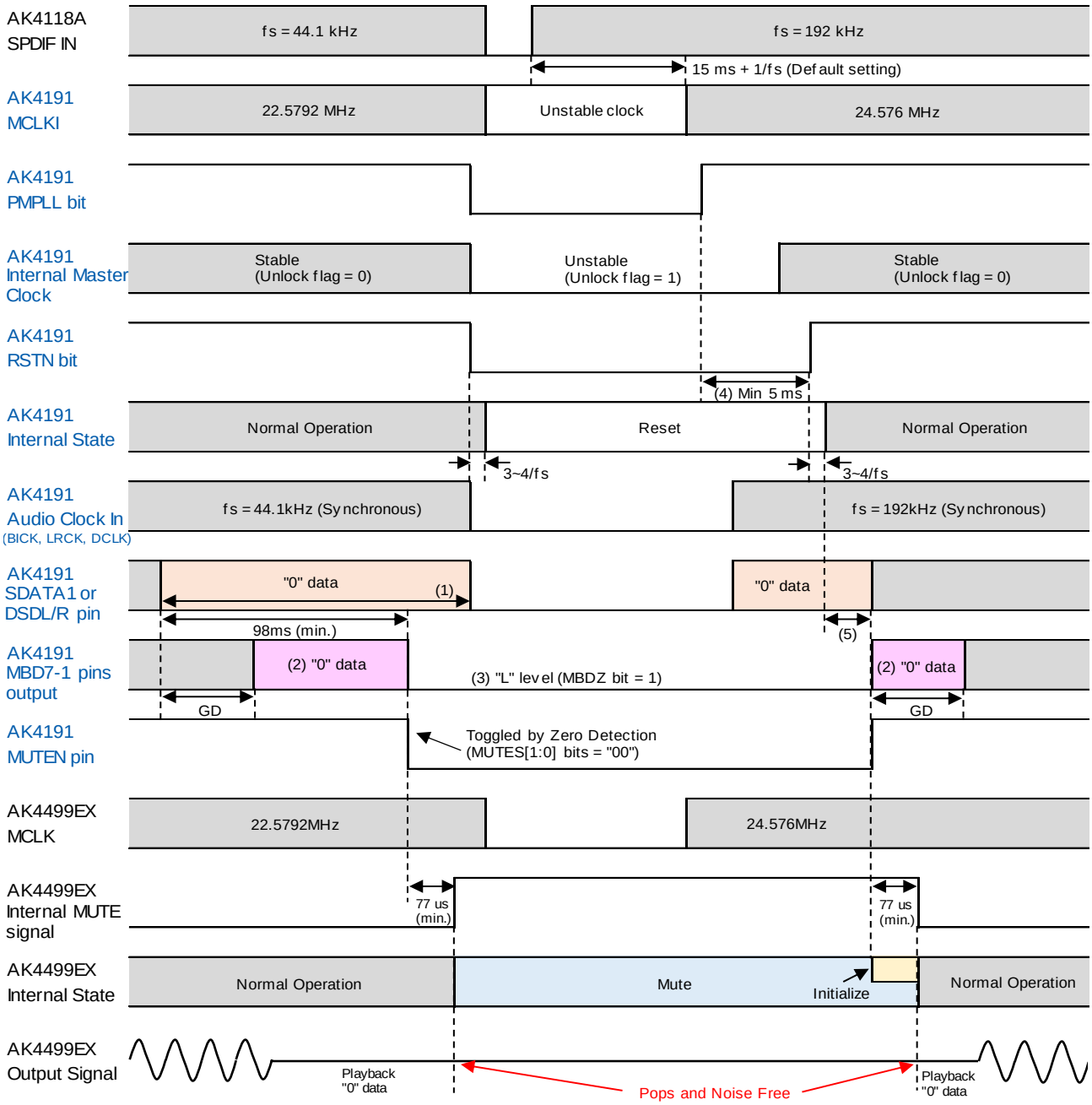


Figure 7. Clicks and Pops free switching sequence example using AK4191 in synchronous mode with DIR

Notes:

(1) It is recommended that data zero input in AK4191 is held until internal MUTE signal of AK4499EX goes to “L” to avoid Clicks and Pops free mode switching (min. 4096 * 256 / FCKB + 77 [us]).

(2) MBD7-1 outputs Delta-Sigma’s zero data with out-of-band noise.

(3) The AK4191 has Delta Sigma Modulator Data zero output function. This function is enabled by setting MBDZ bit = ”1”. MBD1-7 pins go to “L” when MUTEN pin outputs “L”.

(4) RSTN bit should be set to “1” with an interval of 5 ms (min.) for stabilization of PLL circuit after clock reset is released.

(5) It is recommended that data zero input in AK4191 is held 77 us (min.) after Internal reset state of AK4191 is released.

6. POP noise free solution

The AK4191 generates MUTEN signal to control the AK4499EX and avoid noise that occurs when switching audio sources or in abnormal conditions. Therefore, POP noise can be suppressed by simply connecting #33 MUTEN pin of the AK4191 and #16 MUTEN pin of the AK4499EX and controlling the AK4191. Figure 8 shows conditions under which MUTEN signal goes “L”. It is possible to change conditions to generate MUTEN signal by setting MUTES[1:0] bits.

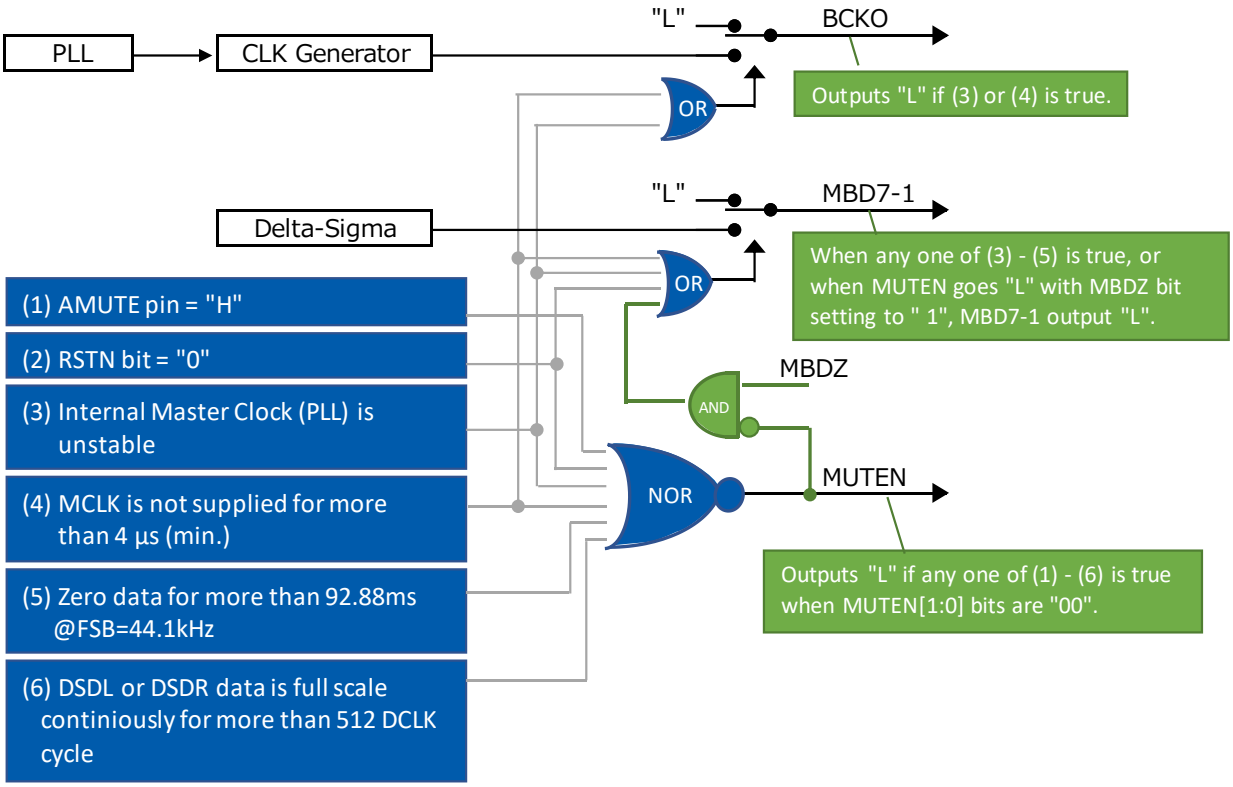


Figure 8. Conditions under which MUTEN signal goes “L”

Notes;

(1) When AMUTE signal via #18 pin goes “H”, MUTEN signal immediately goes “L”. If a flag indicating an abnormal state such as the PLL unlock flag of the Audio Source Device to #18 AMUTE pin of the AK4191, it can directly control the AK4499EX and set MUTE state in abnormal conditions.

(2) When RSTN bit is set “0”, MUTEN signal immediately goes “L”. It is recommended to set RSTN bit “0” when switching audio sources to avoid noise and operate the proper mode.

(3) The AK4191 integrates PLL and generates Internal Master Clock from MCLKI input via #59 MCLK pin. When Internal Master Clock is unstable, the AK4191 generates UNLOCK flag internally and set MUTEN signal “L”. In this condition, BCKO via #46 pin goes “L”. It is recommended to set PMPLL bit “0” when switching MCLKI frequency.

(4) When MCLKI is not supplied for more than 4us (min.), MUTEN signal immediately goes “L”. In this condition, BCKO via #46 pin goes “L”. It is recommended to set PMPLL bit “0” when switching MCLKI frequency.

(5) When data of both channels is continuously “0” for more than 92.88ms (@FSB=441.kHz), MUTEN signal immediately goes “L”. In this case, MBD7-1 outputs Delta-Sigma’s zero data with out-of-band noise, but MBD7-1 outputs “L” by setting MBDZ bit “1”.

(6) Either L channel or R channel DSD data is full scale continiously for more than 512 DCLK cycle (when setting DDMT bit “0”), MUTEN signal goes “L”. In this case, DSD data is forced zero automatically by setting DDM bit = “1”, and avoid POP noise.

--- Refer to following section in the AK4191 datasheet.
- --- 9.8. Zero Detection, DSD Full-scale Detection
- --- 9.12. MUTEN output
- --- 9.13. Delta Sigma Modulator Data zero output

7. Design of Analog Output Post-Circuit

This chapter explains the operating conditions of the AK4499EX external output I-V Conversion Circuit. Op-amp selection, the output signal level, the output signal DC level, cut-off frequency and signal summation are discussed regarding IOUT and OPIN pins.

7.1. I-V Conversion Circuit Overview

The AK4499EX analog outputs are fully differential. The full-scale output at each IOUTx pin is 36.4 mA pk-pk typically. Each output current is converted to voltage by an external I-V conversion circuit. The common output voltage of each AK4499EX IOUTx pin is nominally *Voff'*, but the output signal common mode voltage at the output of each I-V output stage is *Vdcbias*, which can be adjusted if desired. If *Vdcbias* is adjusted by the circuit designer, then *Voff'* is determined by the AK4499EX output impedance, typically 110 Ω, and the value of Rfb. By virtue of changing the *Voff'* operating condition, the "Voff Circuit" output voltage, Voff, must also be changed, by changing the resistor divider values, so that the Voff = *Voff'*

The output range of each I-V conversion path is 4.6 Vrms, centered around the output signal common voltage, and 9.2 Vrms after differential summing. Each output current from the IOUTP and IOUTN pins current should not be summed. Instead, the differential output voltages after the I-V conversion, should be summed externally.

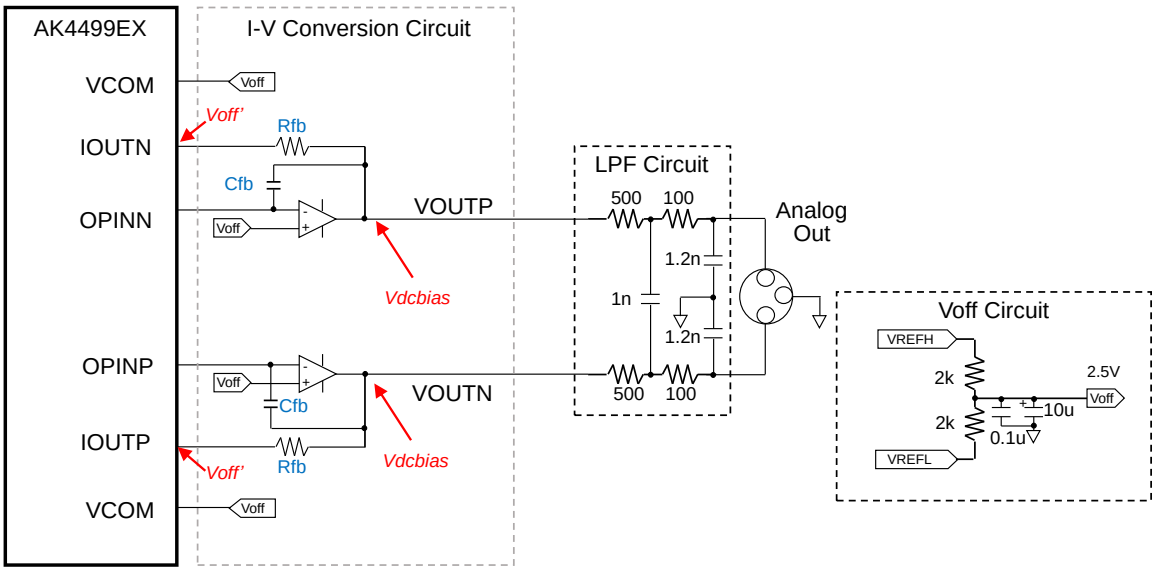


Figure 9. Recommend External I-V Conversion Circuit (*Vdcbias* = 2.5V)

Notes:

(1) Input voltage range of the operational amplifier for I-V conversion circuit is from 0.5 V (typ.) to 2.5 V (typ.). The signal common voltage (VOUTLP and VOUTLN) does not have to be 0 V.

(2) Resistors used in the I-V conversion circuit are recommended to be within 0.1% of absolute error in order to meet specifications.

7.2. I-V Conversion op-amp selection

OPA1611 or OPA1612 are recommended for I/V conversion circuit in view of Gain-Bandwidth, Slew Rate and Input Voltage Noise Density.

Table 5. Key Specifications for Op-Amp

Brand	Parts No.	GBW [MHz]	Slew Rate [V/μs]	Noise [nV/√Hz]	THD [dB]	Output Current [mA]
TI	OPA1611/12	40	27	1.1	-136	35

Guide:
We have tested OPA1611 and we can achieve good S/N and THD values when connected to the AK4499EX. Other op-amp may also be suitable, but we recommend five static specifications listed in Table 5 should be similar or improved.

7.3. Rfb resistor value and output level relation

AK4499EX peak current at +full-scale output is shown in below formula.

IOUTP = 36.4 [mApp]
IOUTN = -36.4 [mApp]

Output signal of I-V Conversion Circuit is decided by below formula.

VOUTP − VOUTN = IOUTP × Rfb − IOUTN × Rfb

Example, in case Rfb is 360 [Ω],

VOUTP − VOUTN = 36.4 [mApp] × 360 [Ω] – (-36.4 [mApp] × 360 [Ω])
= 26.2 [Vpp]
= 9.2 [Vrms]

7.4. Common voltage of Voff and I/V Conversion Circuit output

Voff' = offset voltage of the AK4499EX analog signal.
Vdcbias = *Vdcbias* is signal DC voltage after the I-V conversion circuit.

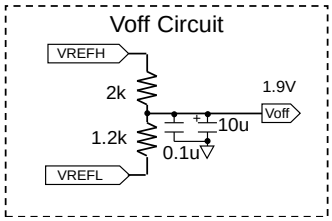
$$\frac{2.5V - Voff'}{110\Omega} = \frac{Voff' - Vdcbias}{Rfb}$$

Premises for this formula,
VREFH = 5V, VREFL = 0V (2.5V is internally determined inside the AK4499EX).
Left side is shown the current from AK4499EX. 110 Ω is AK4499EX output impedance. Right side is shown the current from I/V Conversion Circuit to Rfb resistor.

Example; We choose Rfb to be 360 Ω and we desire *Vdcbias* = 0 V (Grand Center Signal)

$$\frac{2.5V - Voff}{110\Omega} = \frac{Voff - 0}{360\Omega}$$

Therefore, *Voff'* = VCOM = 1.914V.
(Note - AK4499EX VCOM is an input pin).



In this case, the Voff Circuit resistor divider requires changing to 2kΩ and 1.2kΩ.

7.5. Cfb and cut off frequency of I/V Conversion Circuit output

Cut off frequency fc is shown in below formula.

$$fc = \frac{1}{2 \times \pi \times Rfb \times Cfb}$$

Example; In case Rfb is 360 Ω. AKM recommends 180pF for Cfb capacitance.

$$fc = \frac{1}{2 \times \pi \times Rfb \times Cfb} = \frac{1}{2 \times \pi \times 360\Omega \times 180pF} = 2.4MHz$$

7.6. Current summing IOUTP or IOUTN

We do not recommend current summing of any IOUT pins because a mismatch in the I/V conversion circuit for each IOUT pins can incur significant distortions of the output signal. Therefore, we recommend voltage summing, after the I/V Conversion Circuit.

7.7. Regarding IOUTP and IOUTN outputs

AK4499EX has analog output pins that are “P” and “N”. Detail is shown in below.

■Feedback Loop of External I-V Operational Amplifier

Figure 10 shows the internal status of the AK4499EX when the analog output is Hi-Z (PDN = L, PW1/2 = L, or audio clocks stopped) and when the analog output is idle (reset state). The feedback loop of the external amplifier is always maintained while the power supply of the AK4499EX is on.

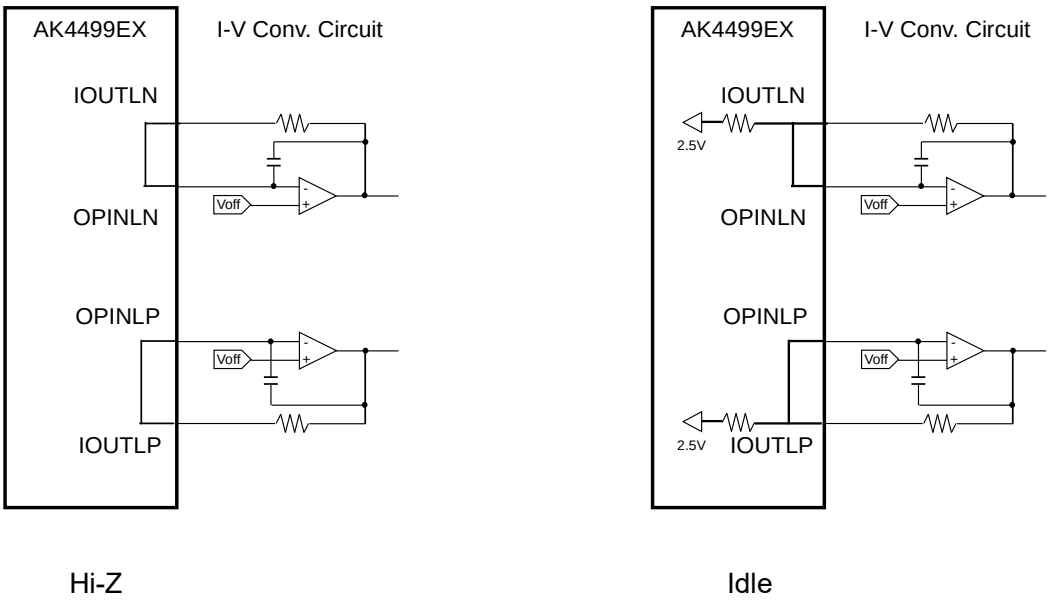


Figure 10. Internal Status of the AK4499EX when Outputting Hi-Z or Idle

7.8. Circuit example of V-I conversion

AKM original circuit output 13.1V pk-pk signal. Output current Ic is estimated below formula.

$$Ic = \frac{13.1Vpp}{Rvi} \ [A]$$

In the case that each IOUTx/OPINx output generates 13.1V pk-pk at the IV stage o/p, by virtue of the calculate in section 7.3.

When Rvi is 1.31kΩ, Ic is 10mA.

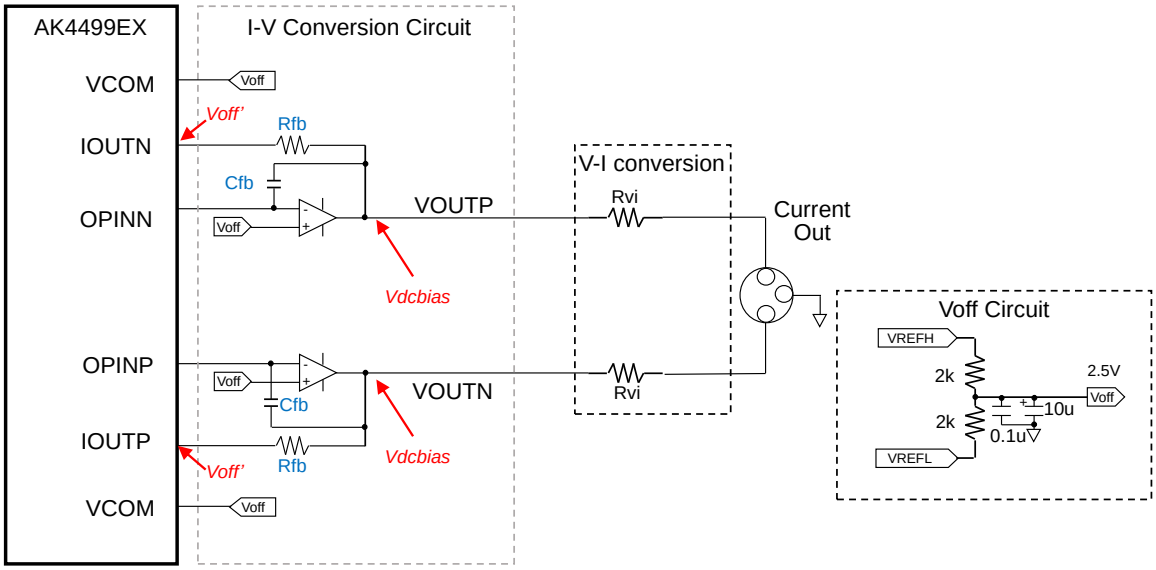


Figure 11. Example circuit of I-V Conversion (*Vdcbias* = 2.5V)

8. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
22/06/06	00	First Edition		

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