AKD4499EX-A

AK4499EX Evaluation Board Rev.0

1. General Description

The AKD4499EX-A is an evaluation board for the AK4499EX (Premium 32-bit 2ch stereo DAC) that supports Network-Audios, USB-DAC, Car-Audio Systems. It integrates differential output low pass filters, allowing quick evaluation with digital audio interface.

■ Ordering Guide

AKD4499EX-A -- Evaluation Board for the AK4499EX
(A USB I/F board for IBM-AT compatible computers and control software are included in this package.)

2. Function

- **Low Pass Filters (LPF) for Pre-amplifier Outputs**
- **Digital Audio Interface (AK4118A)**
- **10-pin Header for Serial Control (AK4499EX / AK4191 / AK4118A)**
- **64-bit Stereo Digital Delta-Sigma Modulator (AK4191)**

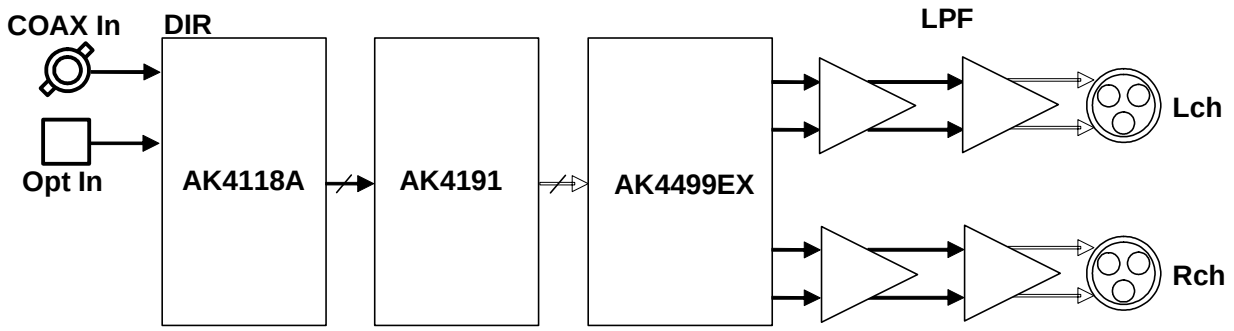


Figure 1. AKD4499EX-A Block Diagram (Note 1)

Note 1. Circuit schematics are attached at the end of this document.

3. Board Appearance

■ Appearance Diagram

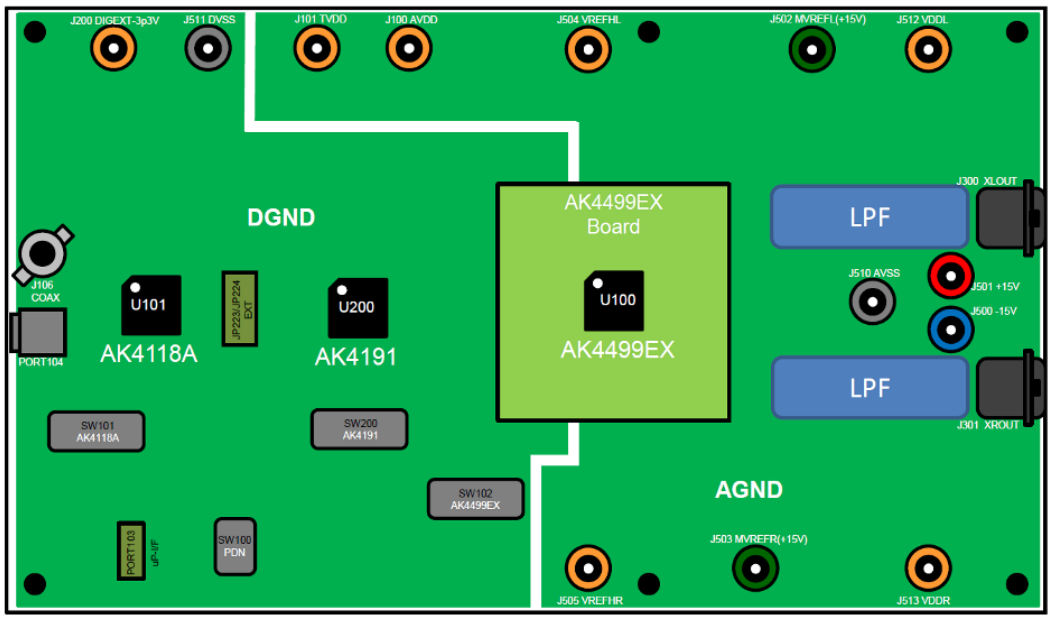


Figure 2. AKD4499EX-A Outline View

■ Description

(1) Connectors for Power Supply and GND
(J501/J500/J100/J101/J512/J513/J504/J505/J502/J503/J510/J511/J200)
(+15V, -15V, AVDD, TVDD, VDDL, VDDR, VREFHL, VREFHR, MVREFL(+15V), MVREFR(+15V), AVSS, DVSS, DIGEXT-3p3V)
Connectors for power supply and the ground
Refer to the “Power Supply Connections” for details.

(2) SPDIF Input Connectors (J106 / BNC Connector, PORT104 / Optical Connector)
Input a SPDIF signal to the AK4118A.
Set the JP108 jumper pin to ‘Up’ side when using the J106 (BNC Connector) jack.
Set the JP108 jumper pin to ‘Down’ side when using the PORT104 (Optical Connector).

(3) Analog Output Terminals (J300 / J301, XLR Connector)
Differential Analog Output Connector

(4) AK4499EX (PCB mounted on CN1, CN2, CN3 and CN4 connectors.)
The AK4499EX is a premium 32-bit 2ch DAC.
Board: AKD4499EX-A-SUB-64HTQFP

(5) AK4191 (U200)
The AK4191 is a 64-bit Stereo Digital Delta-Sigma Modulator for the AK449X (Multi-bit DAC) .

(6) AK4118A (U101)
The AK4118A is a digital audio transceiver.
It is used when evaluating sound quality of the AK4499EX by SPDIF signals.

(7) µP-IF PORT (PORT103)
10-pin Header for the USB I/F board for AK4499EX and the AK4191 and the AK4118A.
Connect the USB I/F board for IBM-AT compatible computers to this port for a connection to a USB port of a PC. Refer to the “Serial Control Mode” for details.

(8) DIP Switches
(Main Board : SW101 / SW102 / SW200)
Setting Switches for the AK4499EX and the AK4191 and the AK4118A.
Upside is “H” (ON) and Downside is “L” (OFF).
Refer to “■ Jumper Pin and DIP Switch Settings” for details.

(9) Toggle Switch (Main Board: SW100)
Setting Switches for the AK4499EX and the AK4191 and the AK4118A.
Upside is “H” (ON) and Downside is “L” (OFF).

4. Operation Sequence

■ **Operation sequence**

1). Power Supply Connections
2). Evaluation Mode
3). Jumper Pin and DIP Switch Settings
4). Power-up
5). Register control (Serial control)

■ Power Supply Connections

No.	Name	Voltage	Content	Note	Default Setting
J501	+15V	+10 to +15V	MVDD+ (Regulator), Op-Amp	This jack is always needed.	+15V
J500	-15V	-10 to -15V	Op-Amp	This jack is always needed.	-15V
J502	MVREFL(+15V)	+10 to +15V	MVREFL (Regulator for AK4499EX)	These are used when supplying MVREFL/R(+15V) from a MVREF connector for a regulator. Set the JP509 and JP510 jumper pins to "MVREF" side.	Open
J503	MVREFR(+15V)	+10 to +15V	MVREFR (Regulator for AK4499EX)		Open
J101	TVDD	+1.7 to +3.6V	TVDD (AK4499EX)	These are used when supplying TVDD, AVDD, VDDL and VDDR from a 1.8V or a 3.3V or a +5V or a EXT connector without a regulator. Set the JP100 and JP101 jumper pins to "REG(5.0V)" side and "REG(3.3V)" side. Set the JP505 and JP506 jumper pins to "+5V" side.	Open
J100	AVDD	+4.75 to +5.25V	AVDD (AK4499EX)		Open
J512	VDDL	+4.75 to +5.25V	VDDL (AK4499EX)		+5V
J513	VDDR	+4.75 to +5.25V	VDDR (AK4499EX)		+5V
J504	VREFHL	+4.75 to +5.25V	VREFHL (AK4499EX)	These are used when supplying VREFHL/R from a +5V connector without a regulator. Set the JP501 and JP502 jumper pins to "+5V" side.	Open
J505	VREFHR	+4.75 to +5.25V	VREFHR (AK4499EX)		Open
J200	DIGEXT-3p3V	+2.7 to +3.6V	TVDD1,TVDD2,PVDD, TVDD3,TVDD4 (+3.3V for AK4191) Regulator(T201,T202) (+1.8V or +1.2V for AK4191)	These are used when supplying TVDD1,TVDD2,PVDD,TVDD3,TVDD4 from a +3.3V connector without a regulator. Set the JP210 jumper pins to "EXT(3.3V)" side.	Open
J510	AVSS	0V	Analog Ground	This jack is always needed.	0V
J511	DVSS	0V	Digital Ground	This jack is always needed.	0V

Table 2. Power Supply Connections (Note 2)

Note 2. Each power supply line should be distributed separately from the power supply unit.

■ Evaluation Mode

(1) Evaluation with a DIR (COAX) < Default >

The J106 (COAX) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the J106 (COAX) connector.
Set the JP108 (RX-SEL) jumper pin to 'Up' side (3pin"BNC") , and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open', and set the JP220 (MCLKI) jumper pin to 'DIR/EXT short and Xtal open'.

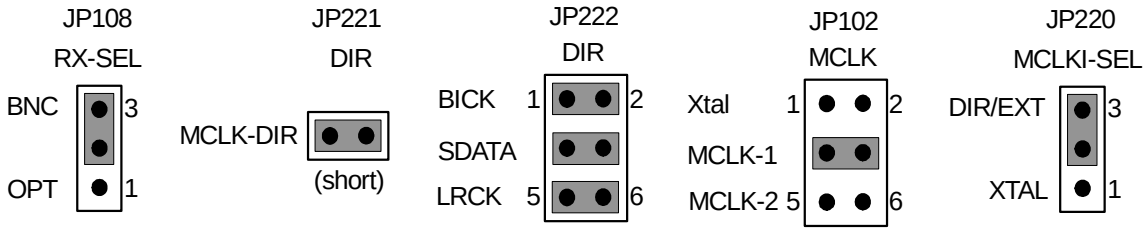


Figure 3. Jumper Pin Settings with DIR

(2) Evaluation with a DIR (OPTICAL)

The PORT104 (OPTICAL) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the PORT104 (OPTICAL) connector.
Set the JP108 (RX-SEL) jumper pin to 'Down' side (1pin"OPT") , and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open', and set the JP220 (MCLKI) jumper pin to 'DIR/EXT short and Xtal open'.

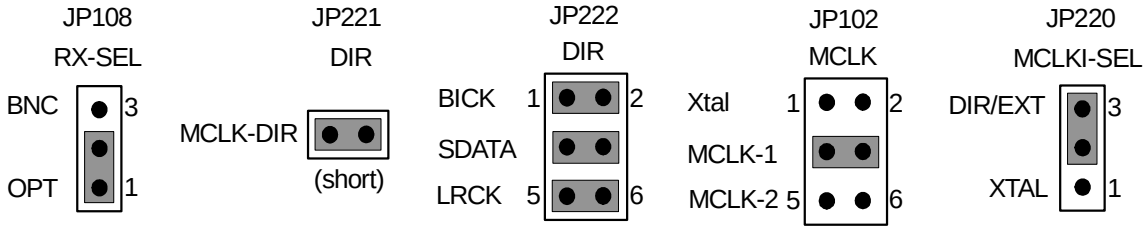


Figure 4. Jumper Pin Settings with DIR

(3) In the case that all interface clocks including the master clock are input externally. (JP223, JP224)

Input all interface clocks including the master clock to the JP223 and JP224.
The JP223 (EXT for MCLK) and the JP224 (EXT for BICK and SDATA and LRCK) jumper ports is used in this mode.
MCLK from the input master clock of the JP223 2pin.
Set the JP221 (DIR: MCLK) jumper pin to 'open'.
BICK, LRCK and SDATA from the input data of the JP224 2pin, 4pin and 6pin.
Set the JP222 (DIR: BICK, SDATA, LRCK) jumper pin to 'open'.

External master clock input :

JP223 : MCLK

Signal	Pin No.		Signal
VSS or open	1	2	MCLK

Note. Jumper settings for JP223. : open

External data and clock input :

JP224 : BICK, SDATA, LRCK

Signal	Pin No.		Signal
VSS or open	1	2	BICK
VSS or open	3	4	SDATA
VSS or open	5	6	LRCK

Note. Jumper settings for JP224. : open

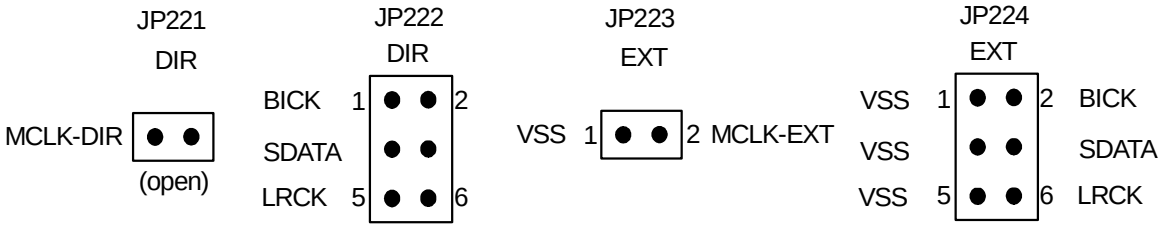


Figure 5. Jumper Pin Settings with External Clocks

■ Jumper Pin and DIP Switch Settings

(1) Jumper Pin Settings

Table 3-1-1. Jumper Settings for power supply [**Main Board**]

No.	Name	Content	Default Setting
JP100	AVDD	AVDD pin input select REG(3.3V): The AVDD pin is supplied from the T100 regulator. REG(1.8V): The AVDD pin is supplied from the T104 regulator. EXT: The AVDD pin is supplied from the J100 (AVDD) connector.	REG(5.0V)
JP101	TVDD	TVDD pin input select REG(3.3V): The TVDD pin is supplied from the T101 regulator. REG(1.8V): The TVDD pin is supplied from the T105 regulator. EXT: The TVDD pin is supplied from the J101 (TVDD) connector.	REG(3.3V)
JP501	VREFHL	VREFHL pin input select REG: The VREFHL pin is supplied from the VREFHL regulator. +5V: The VREFHL pin is supplied from the J504 (VREFHL) connector.	REG
JP502	VREFHR	VREFHR1 pin input select REG: The VREFHR pin is supplied from the VREFHR regulator. +5V: The VREFHR pin is supplied from the J505 (VREFHR) connector.	REG
JP509	MVREFL(+15V)	MVREFL(+15V) power supply for VREFHL1 regulator input select MVDD+: The power supply (MVREFL) for VREFHL1 regulator is supplied from the J501 (+15V) connector. MVREF: The power supply (MVREFL) for VREFHL1 regulator is supplied from the J502 (MVREFL(+15V)) connector.	MVDD+
JP510	MVREFR(+15V)	MVREFR(+15V) power supply for VREFHR1 regulator input select MVDD+: The power supply (MVREFR) for VREFHR1 regulator is supplied from the J501 (+15V) connector. MVREF: The power supply (MVREFR) for VREFHR1 regulator is supplied from the J503 (MVREFR(+15V)) connector.	MVDD+
JP505	VDDL	VDDL pin input select REG: The VDDL pin is supplied from the T500 regulator. +5V: The VDDL pin is supplied from the J512 (VDDL) connector.	+5V
JP506	VDDR	VDDR pin input select REG: The VDDR pin is supplied from the T501 regulator. +5V: The VDDR pin is supplied from the J513 (VDDR) connector.	+5V
JP500	VSS-SEL1	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open
JP520	VSS-SEL2	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open

JP550	VSS-SEL3	Connection between Analog VSS pattern and Digital VSS pattern. Solder short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open
JP551	VSS-SEL4	Connection between Analog VSS pattern and Digital VSS pattern. Solder short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open
JP210	DIGVDD1	DIGVDD1 power supply for VDD (the AK4191) regulator output select. REG(3.3V): The DIGVDD1 pin is supplied from the T200 regulator. EXT(3.3V): The DIGVDD1 pin is supplied from the J200 connector. (DIGEXT-3p3V)	REG(3.3V)
JP211	TVDD1	TVDD1 power supply for VDD (the AK4191) regulator output select. REG(3.3V): The TVDD1 pin is supplied from the JP210 connector pin. REG(1.8V): The TVDD1 pin is supplied from the T201 regulator.	REG(3.3V)
JP212	TVDD2	TVDD2 power supply for VDD (the AK4191) regulator output select. REG(3.3V): The TVDD2 pin is supplied from the JP210 connector pin. REG(1.8V): The TVDD2 pin is supplied from the T202 regulator.	REG(3.3V)
JP213	TVDD3	TVDD3 power supply for VDD (the AK4191) regulator output select. REG(3.3V): The TVDD3 pin is supplied from the JP218 connector pin. REG(1.8V): The TVDD3 pin is supplied from the T203 regulator.	REG(3.3V)
JP214	TVDD4	TVDD4 power supply for VDD (the AK4191) regulator output select. REG(3.3V): The TVDD4 pin is supplied from the JP218 connector pin. REG(1.8V): The TVDD4 pin is supplied from the T204 regulator.	REG(3.3V)
JP215	DVDD	DVDD power supply for VDD (the AK4191) regulator output select. REG(1.2V): The DVDD pin is supplied from the T205 regulator.	REG(1.2V)
JP216	PVDD	PVDD power supply for VDD (the AK4191) regulator output select. REG(3.3V): The PVDD pin is supplied from JP210 connector pin.	REG(3.3V)
JP217	SWVDD	SWVDD power supply for VDD (the SW200) regulator output select. REG(3.3V): The SWVDD pin is supplied from JP210 connector pin.	REG(3.3V)

Table 3-2-1. Jumper Settings for data & clock [**Main Board**]

No.	Name	Content	Default Setting
JP108	RX-SEL	SPDIF signal for AK4118A Upside: SPDIF signal is supplied from the J106 (COAX) connector. Downside: SPDIF signal is supplied from the PORT104 (Optical) connector.	Up side (BNC)

JP102	MCLK	MCLK pin (AK4499EX) input select MCLK-1 3pin-4pin short: MCLK-1 signal is supplied from the DIR (AK4118A) (JP221) or the external clock (JP223). MCLK-2 5pin-6pin short: MCLK-2 signal is supplied from U200 (MCLKO). Xtal 1pin-2pin short: Xtal MCLK signal is supplied from the crystal oscillator output.	MCLK-1 short
JP103	MUTEN-SW	MUTEN pin (AK4499EX) input select short: MUTEN signal is supplied from the DIP-SW (SW102-4pin). open: MUTEN signal is supplied from JP103-1pin (external signal).	short
JP220	MCLKI-SEL	MCLKI pin (AK4191) input select DIR/EXT 3pin-2pin short: DIR/EXT signal is supplied from the DIR (AK4118A) (JP221) or the external clock (JP223). Xtal 1pin-2pin short: Xtal MCLK signal is supplied from the crystal oscillator output.	DIR/EXT short
JP221	MCLK-DIR	MCLK pin from DIR (AK4118A) output select short: MCLK signal is supplied from the DIR (AK4118A). open: MCLK signal is open.	short
JP222	BICK-DIR SDATA-DIR LRCK-DIR	DATA (BICK, SDATA, LRCK) pins from DIR (AK4118A) output select short: DATA signals are supplied from the DIR (AK4118A). open: DATA signals are open.	short

Table 3-3. Chip resistor Settings for control signal [**Sub Board : AKD4499EX-A-SUB-64HTQFP**]

No.	Name	Content	Default Setting
R111 R112	CSN OSR	OSR/CSL pin input select CSN: This setting is for Serial Control Mode. OSR: This setting is for Parallel Control Mode. (Parallel Control setting by Main Board SW102)	CSL R111: short R112: open
R113 R114	CCLK/SCL LRSEL0	LRSEL0/CCLK/SCL pin input select CCLK: This setting is for Serial Control Mode. LRSEL0: This setting is for Parallel Control Mode. (Parallel Control setting by Main Board SW102)	CCLK/SCL R113: short R114: open
R115 R116	CDTI/SDA LRSEL1	LRSEL1/CDTI/SDA pin input select CDTI: This setting is for Serial Control Mode. LRSEL1: This setting is for Parallel Control Mode. (Parallel Control setting by Main Board SW102)	CDTI/SDA R115: short R116: open

(2) DIP Switch Setting
Upside is ON (“H”), and Downside is OFF (“L”).

AK4118A Settings : Main Board

[SW101]: Setting of the AK4118A

No.	Name	ON (“H”)	OFF (“L”)	Default
1	PSN	Parallel Control Mode	Serial Control Mode	H
2	DIF2	Audio I/F Format for AK4118A Refer to **Table 4-1-1.**		H
3	DIF1			L
4	DIF0			H
5	OCKS1	Master Clock setting for AK4118A Refer to **Table 4-1-2.**		H
6	OCKS0			L
7	CAD1	CAD1 pin = “H”	CAD1 pin = “L”	H
8	CAD0	CAD0 pin = “H”	CAD0 pin = “L”	L

Table 4-1. SW101 Setting (AK4118A)

Mode	DIF2 pin	DIF1 pin	DIF0 pin	SDTO	LRCK		BICK		
0	L	L	L	16bit Right justified	H/L	O	64fs	O	
1	L	L	H	18bit Right justified	H/L	O	64fs	O	
2	L	H	L	20bit Right justified	H/L	O	64fs	O	
3	L	H	H	24bit Right justified	H/L	O	64fs	O	
4	H	L	L	24bit Left justified	H/L	O	64fs	O	
5	H	L	H	24bit I2S	L/H	O	64fs	O	< Default >
6	H	H	L	24bit Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit I2S	L/H	I	64-128fs	I	

Table 4-1-1. Audio I/F Format of the AK4118A

Mode	OCKS1	OCKS0	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	< Default >
3	H	H	128fs	192 kHz	

Table 4-1-2. Master Clock Setting of the AK4118A

AK4499EX Settings : Main Board

[SW102]: Setting of the AK4499EX

No.	Name	ON (“H”)	OFF (“L”)	Default
1	OSR	(In Parallel Control Mode) Operating rate is 5.6MHz (44.1kHz *128)	(In Parallel Control Mode) Operating rate is 11.2MHz (44.1kHz *256)	H
2	LRSEL0	(In Parallel Control Mode) Stero/Mono mode Select, Output Signal Select		L
		LRSEL0 pin = H	LRSEL0 pin = L	
3	LRSEL1	(In Parallel Control Mode) Stero/Mono mode Select, Output Signal Select		L
		LRSEL1 pin = H	LRSEL1 pin = L	
4	MUTEN	Mute “OFF” Normal Operation	Mute “ON” Mute Mode	H
5	HOLD1/CAD0	(In Parallel Control Mode)	(In Parallel Control Mode)	H
		CAD0 pin = “H”	CAD0 pin = “L”	
6	TST1/CAD1	TST1 = H (In Parallel Control Mode)	TST1 = L (In Parallel Control Mode)	L
		CAD1 pin = “H” (In Serial Control Mode)	CAD1 pin = “L” (In Serial Control Mode)	
7	PSN	Parallel Control Mode	Serial Control Mode	L
8	VTSEL/I2C	VTSEL pin = H (In Parallel Control Mode)	VTSEL pin = L (In Parallel Control Mode)	H
		I2C-Bus Control mode (In Serial Control Mode)	3-wire Serial Control mode (In Serial Control Mode)	
9	NC	-	-	L
10	NC	-	-	L

Table 4-2. SW102 Setting (AK4499EX)

AK4191 Settings : Main Board

[SW200]: Setting of the AK4191

No.	Name	ON (“H”)	OFF (“L”)	Default
1	I2C	Serial Control Interface Select pin in Register control mode.		H
		I2C Bus serial control interface	4-wire serial control interface	
2	CAD1	Chip Address pins in Register control mode. CAD1 : Chip Address 1. CAD0 : Chip Address 0.		L
3	CAD0			L
4	PROG	Programmable Filter Coefficient Setting Enable		L
		I2C=”L”: Programmable Filter Coefficients Memory Access Mode I2C=”H”: Not Available	Resister Control Access Mode	
5	AMUTE	Mute Control in Parallel control mode.		L
		Mute cycle: MUTEN=”L”	Usually Mute releases: MUTEN=”H” However, depending on other conditions, it may be Mute releases or Mute cycle.	
6	TEST2	Test Mode Enable Pin. Connect to DVSS.		L
7	TEST1			L
8	NC	-		L
9	NC	-		L
10	NC	-		L

Table 4-3. SW200 Setting (AK4191)

■ Power-up

Upside is ON (“H”), and Downside is OFF (“L”).

[SW100] (PDN): DAC Reset control. It must be set to “H” during operation.
After power-up, the AKD4499EX-A must be reset once.
To reset the AKD4499EX-A, set the SW100 toggle switch to “L” and power down the AK4499EX and the AK4191 and the AK4118A.
Then, release the power-down by setting back the SW100 to “H”.

■ Register control (Serial control)

AKD4499EX-A can be controlled via USB (serial port).

For the AK4499EX and the AK4191 and the AK4118A:
Connect board to PC using the USB cable (PORT103 - serial) included with the AKD4499EX-A.

The control software is packed with the evaluation board.
The software operation sequence is included in the datasheet of each device.

■ Example of evaluation mode:

(1) Normal Mode Sequence : fs=44.1kHz, MCLK=512fs(22.5792MHz), BICK=64fs, 24bit I2S
[Operation rate=OSR128=5.6448MHz, Modulator Data=7bit data mod, GC3-0 bit="0110"]

■ Start up Setting

1: Jumpers and Dip-switches and Toggle-switches are default (Normal Mode) setting.
Note.
Main Board (AK4118A) :
SW101: PSN="H", OCKS1-0="HL" (512fs), DIF2-0="HLH" (24bit I2S)
Main Board (AK4191) :
SW200: I2C=H, CAD1-0="LL", PROG="L", AMUTE="L", TESTE2="L", TESTE1="L"
Sub Board (AK4499EX) :
SW102: OSR="H", LRSEL0="L", LRSEL1="L", MUTEN="H",
CAD1-0="LH", PSN="L", VTSEL/I2C="H"

2: Set the SW100 toggle switch to "L".
Then, release the power-down by setting back the SW100 to "H"

SW100
L→H
AK4499EX, AK4191, AK4118A : Used

Table 5-1. Toggle switch setting

3: Control Soft "ak4191.exe" open.
3-1: Setting : I2C, CAD1-0
3-2: InitPort & Write Default.
3-3: [Script] Tab -> Refer -> "ak4191-defaultset.txt" Load.
Note. The read file (text file) is packed with the evaluation board.

Control Soft for AK4191: RegMap Window (after "Refer")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	DUAL	EXDF	MUTES[1]	MUTES[0]	DIF[2]	DIF[1]	DIF[0]	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset.
0: Reset. All registers are not initialized. (default)
1: Normal Operation

DIF[2:0]: Audio Data Interface modes. Initial value is “110” (Mode 6: 32bit MSB justified).

DIF2/1/0 bit: Set Audio Data Interface Mode for Input Digital Data (Normal Single Mode).
000: 16bit, LSB justified
001: 20bit, LSB justified
010: 24bit, MSB justified
011: 24 or 16bit, I2S compatible
100: 24bit, LSB justified
101: 32bit, LSB justified
110: 32bit, MSB justified
111: 32bit, I2S compatible

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SSLOW	SD	SLOW	DEM[1]	DEM[0]	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

SLOW: Slow Roll-off Filter Enable.
0: Sharp Roll-off filter (default)
1: Slow Roll-off filter
SD: Short Delay Filter Enable.
0: Traditional filter
1: Short Delay filter (default)
SSLOW: Super Slow Roll-off (Digital Filter bypass mode) or Low Dispersion Filter Enable.
0: Disable (default)
1: Enable

SSLOW / SD / SLOW bit: Set Digital Filter Setting (1x/2x/4x/8x/16x speed mode).
000: Sharp Roll-off filter
001: Slow Roll-off filter
010: Short Delay Sharp Roll-off filter
011: Short Delay Slow Roll-off filter
100: Super Slow Roll-off filter
101: Super Slow Roll-off filter
110: Low Dispersion Short Delay filter
111: Programmable filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	ATS [1]	ATS [0]	0	GC [3]	GC [2]	GC [1]	GC [0]	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: SYNC Mode Enable.
0: SYNC mode Disable
1: SYNC mode Enable (default)

GC [3:0]: Gain Control.

ATS [1:0]: Transition Time Between Set Values of ATTL/R [7:0] bits. Initial value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Control 6	BCKS [1]	BCKS [0]	MCKOE	MCKDV	MCKS [1]	MCKS [0]	FS32K	PMPLL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: Power management of PLL
0: PLL off (default)
1: PLL on

FS32K: Sampling Frequency setting.
0: Base Sampling Frequency is 42kHz to 54kHz (default)
1: Base Sampling Frequency is 30kHz to 34kHz

MCKS [1:0]: System Clock Setting. Initial value is "00" (12.288 or 11.2896 MHz).

MCKDV: MCLKO frequency setting. Initial value is "0" (MCLKO frequency is same as MCLK).

MCKOE: MCLKO Output Enable
0: Disable (default)
1: Enable

BCKS[1:0]: BICK/BCK Frequency Setting. Initial value is "00" (128fs).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 7	TDM [1]	TDM [0]	SDS [2]	SDS [1]	SDS [0]	0	OSTME	ISTME
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ISTME: Delta Sigma Modulator Data Input (DSMI) format setting.
0: MONO mode (default)
1: Stereo mode

OSTME: Delta Sigma Modulator Data Output (MBD) format setting.
0: MONO mode (default)
1: Stereo mode

SDS [2:0]: Output Data Slot Selection of Each Channel.

TDM [1:0]: TDM Mode Select.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 8	0	0	0	0	0	0	0	DSYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSYNCE: Data Synchronization Function Setting.
0: Synchronization disable (default)
1: Synchronization enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	DSMI/O	DSMIFS	MBDZ	DSMSEL [1]	DSMSEL [0]	0	OBIT [1]	OBIT [0]	OSR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

OSR: BCKO Frequency Setting. Initial value is "0" (BCKO frequency is 12.288 or 11.2896 MHz).

OBIT [1:0]: Delta Sigma Modulator Data Output (MBD7-1) Bit Number
00: 7 bits (default)

01: 6 bits
10/11: 5 bits

DSMSEL [1:0]: Delta Sigma Modulator Data Output (MBD7-1) Selection Type.
00: Type 1 (default)
01: Type 2
10: Type 3
11: Type 4

MBDZ: Delta Sigma Modulator Data Output (MBD7-1) zero function setting.
0: off (default)
1: force MBD7-1 zero when MUTEN pin outputs “L”.

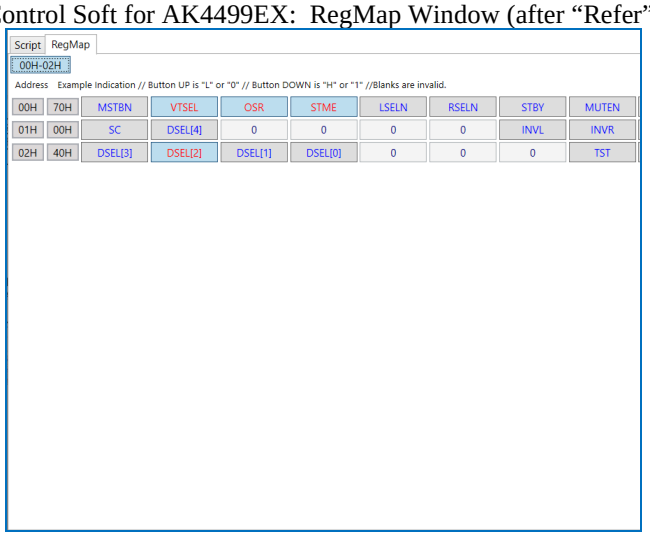
DSMIFS: Delta Sigma Modulator Data Input Frequency (BCKI) Setting.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Reserved	DSEL [7]	DSEL [6]	DSEL [5]	DSEL [4]	DSEL [3]	DSEL [2]	DSEL [1]	DSEL [0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

10H: This address is set to 21H.

4: Control Soft “ak4499ex.exe” open.
4-1: Setting : I2C, CAD1-0
4-2: InitPort & Write Default.
4-3: [Script] Tab -> Refer -> “ak4499ex-defaultset.txt” Load.
Note. The read file (text file) is packed with the evaluation board.
4-4: Setting : MUTEN bit = “1”. (Address 00H: This address is set to 31H.)

Control Soft for AK4499EX: RegMap Window (after “Refer”)



Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control1	MSTBN	VTSEL	OSR	STME	LSELN	RSELN	STBY	MUTEN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MUTEN: The AK4499EX is set in Mute state.
0: Mute. (default)
1: Normal Operation

STBY: Standby ON/OFF control bit
0: Normal Operation (default)
1: Standby

LSELN, RSELN: Input and output combination can be changed by LSELN bit and RSELN bit.

STME: Audio interface format mode select bit.
0: Multi-bit Mono mode (default)
1: Multi-bit Stereo mode

OSR: Sampling speed mode setting bit.
0: OSR256 mode (default)
1: OSR128 mode

VTSEL: VIH/L level select of MCLK bit.
0: VIH=1.36V, VIL=0.34V (default)
1: VIH=2.2V, VIL=0.8V

MSTBN: Stand-by mode by MCLK input enable.
0: enable (default)
1: disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control2	SC	DSEL [4]	0	0	0	0	INVL	INVR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INVL, INVR: The output signal phase can be inverted by INVL bit and INVR bit.

DSEL [4]: “0” value must be written to this bit. Otherwise, malfunction may occur.

SC: Sound control
0: Measurement mode (default)
1: Sound quality mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control3	DSEL [3]	DSEL[2]	DSEL[1]	DSEL[0]	0	0	0	TST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

TST: Test bit. “0” value must be written to this bit. Otherwise, malfunction may occur.

DSEL [3:0]: “0100” value must be written to this bit. Otherwise, malfunction may occur.

■ Serial Control Mode

The AKD4499EX-A (for the AK4499EX) should be connected to a PC (IBM-AT compatible) via a USB control box (AKDUSBIF-B) included in this package. The USB control box is connected to a PC with a USB cable and the AKD4499EX-A with a 10-pin flat cable. (Note.3, Note.4)

Note 3. The AKD4499EX-A accepts only one AKDUSBIF-B at one time. It does not operate if two or more AKDUSBIF-Bs are connected.

Note 4. Connect the 10pin Flat Cable as the red line of the cable is connected to the 1 pin of the 10pin Header of the board.

PORT103 : for the AK4499EX and the AK4191 and the AK4118A

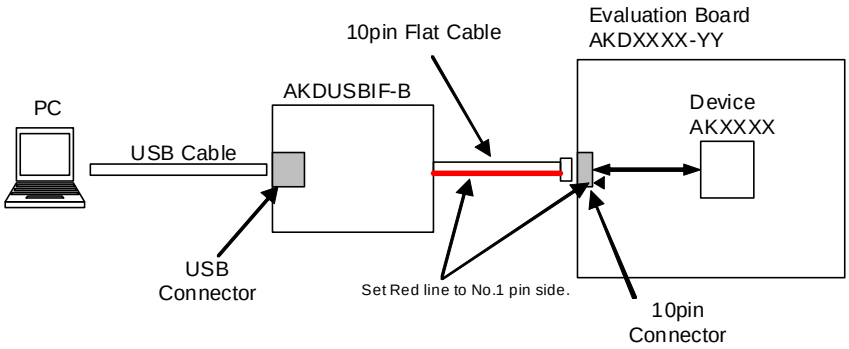


Figure 10. AKDUSBIF-B Connection

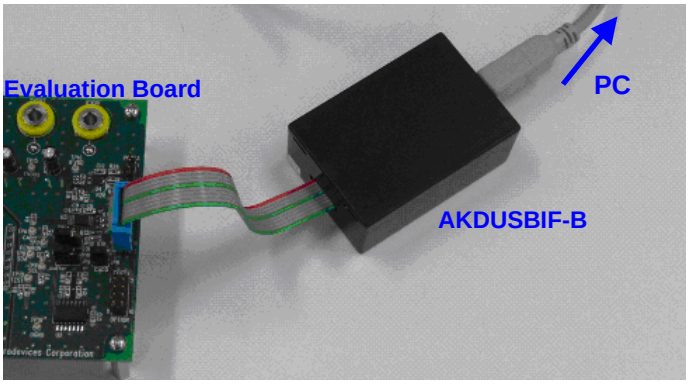


Figure 11. AKDUSBIF-B

Set up the resistor parts. (Control Mode Setting) : For the AK4499EX

Set up the control pins.
CSN: R111=short / R112=open, CCLK/SCL: R113=short / R114=open, CDTI/SDA: R115=short / R116=open

Control Mode settings. ⋯ Selected Position

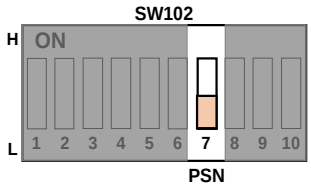
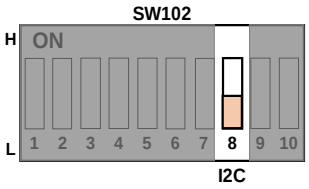
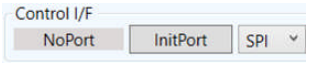
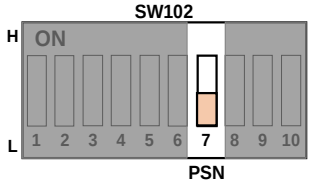
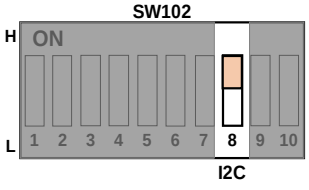
Serial Control Mode	SW102 (AK4499EX) (No.7: PSN)	SW102 (AK4499EX) (No.8 : I2C)	Control Software (Control I/F)
3-wire	 SW102-No.7 = L	 SW102-No.8 = L	
I²C-Bus	 SW102-No.7 = L	 SW102-No.8 = H	

Table 6-1-1. Serial control mode setting

When using this evaluation board in serial control mode, settings of the CAD1 pin and the CAD0 pin on the board must match the Chip Address settings of the control software.

⋯ Selected Position

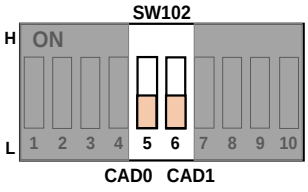
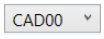
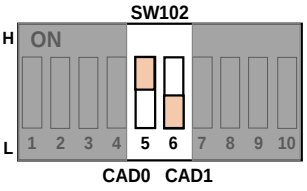
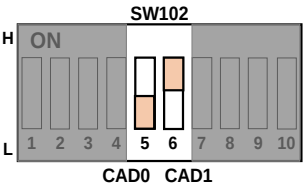
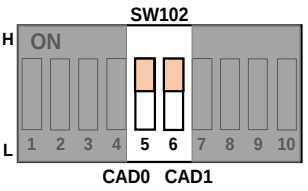
Chip Address	SW102 (AK4499EX) (No.5: CAD0, No.6: CAD1)	Control Software (Chip Address)
"00"	 SW102-No.6 = L , No.5 = L	
"01"	 SW102-No.6 = L , No.5 = H	
"10"	 SW102-No.6 = H , No.5 = L	
"11"	 SW102-No.6 = H , No.5 = H	

Table 6-1-2. "Chip Address" setting

Set up the resistor parts. (Control Mode Setting) : For the AK4191

Control Mode settings. ⋯ Selected Position

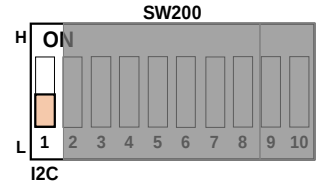
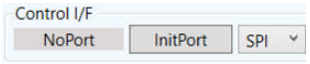
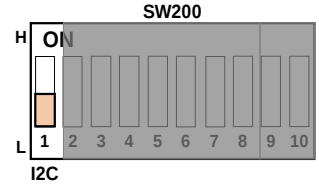
Serial Control Mode	SW200 (AK4191) (No.1 : I2C)	Control Software (Control I/F)
4-wire	 SW200-No.1 = L	
I²C-Bus	 SW200-No.1 = H	

Table 6-1-1. Serial control mode setting

When using this evaluation board in serial control mode, settings of the CAD1 pin and the CAD0 pin on the board must match the Chip Address settings of the control software.

⋯ Selected Position

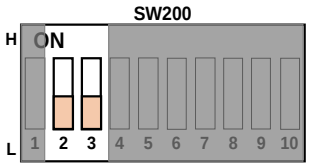
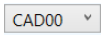
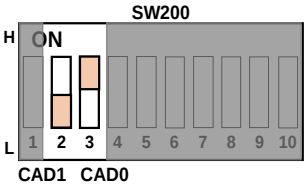
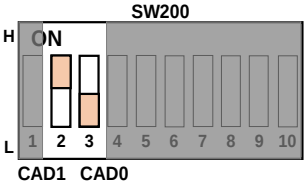
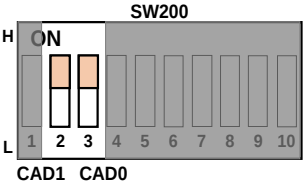
Chip Address	SW200 (AK4191) (No.2: CAD1, No.3: CAD0)	Control Software (Chip Address)
"00"	 SW200-No.2 = L , No.3 = L	
"01"	 SW200-No.2 = L , No.3 = H	
"10"	 SW200-No.2 = H , No.3 = L	
"11"	 SW200-No.2 = H , No.3 = H	

Table 6-1-2. "Chip Address" setting

Control Software Manual

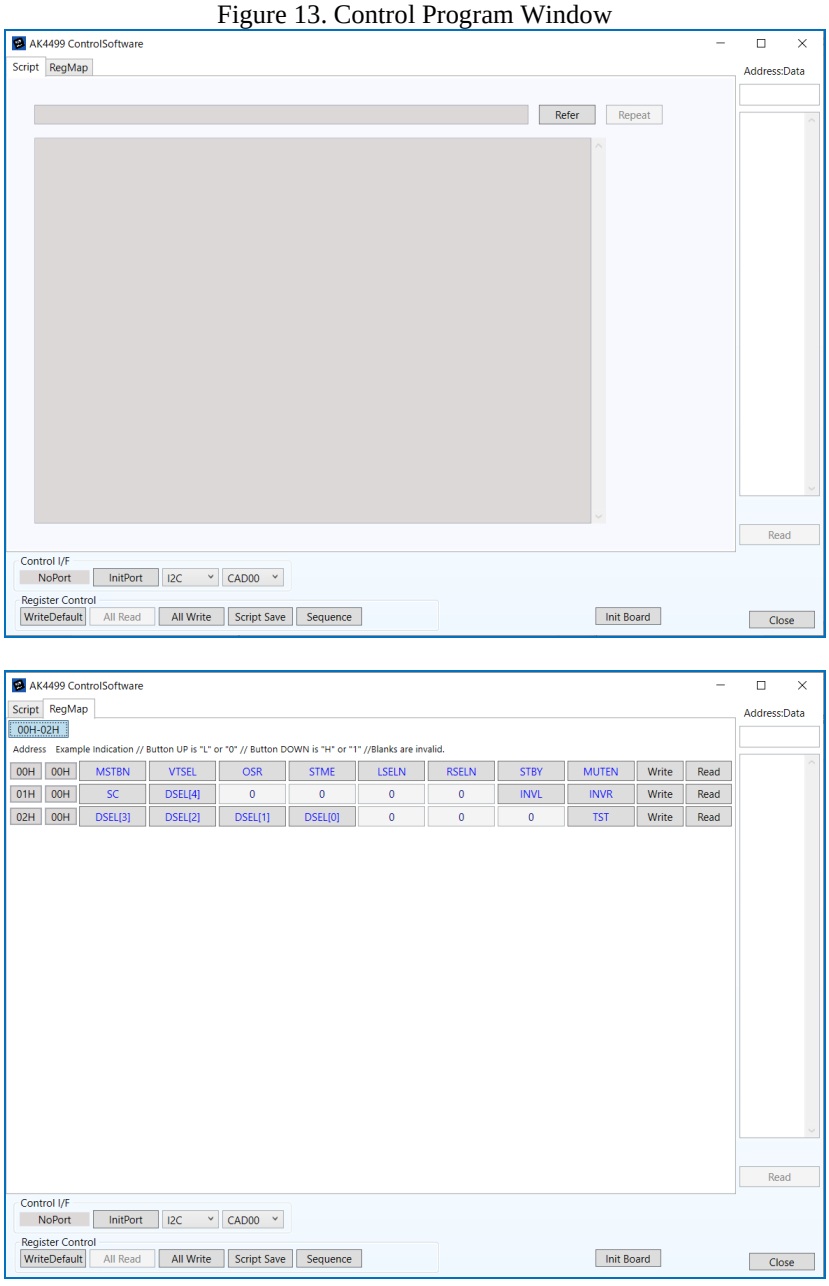
■ Evaluation Board and Control Software Settings

(for the AK4499EX)

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD4499EX-A Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “ak4499ex.exe” to open the control program.
6. Begin evaluation by following the procedure below.

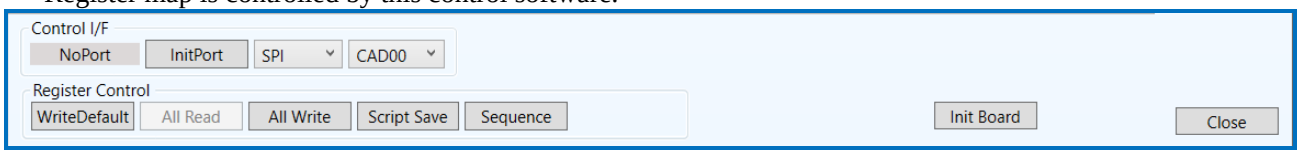
[Supported OS]
Windows 7 (32bit) / Windows 10 (64bit)

Figure 13. Control Program Window



■ Operation Overview

Register map is controlled by this control software.



Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Box” section for details of each dialog box setting.

1.[Init Port]: Reset the USB port.
Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.

2.[SPI / I2C]: Select up interface of the AK4499EX.
This setting can be changed when the PDN pin = “L”.

3.[CAD00 / CAD01 / CAD10 / CAD11]: Select the CAD pin settings.
This setting can be changed when the PDN pin = “L”.

4.[Write Default]: Initialize all registers of the AK4499EX.

5.[All Read]: Executes read commands for all registers displayed. (Note 5)

6.[All Write]: Executes write commands for all registers displayed.

7.[Script Save]: Select a file and save all settings of this software.
The saved file can be used as a script.

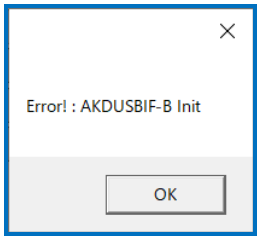
8.[Sequence]: [Sequence] dialog box pops up.

9.[Init Board]: Reset the USB port and the main board.

10.[Close]: Quit the control software.

Note 5. The [All Read] button is only valid when the interface mode for register control is in I^2C bus control mode.

When input dummy command settings to AK4499EX and the connection error by the evaluation board to a PC with USB cable, the following Init error message will pop up. Click “OK”.



■ Tab Functions

1. [RegMap] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.
Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

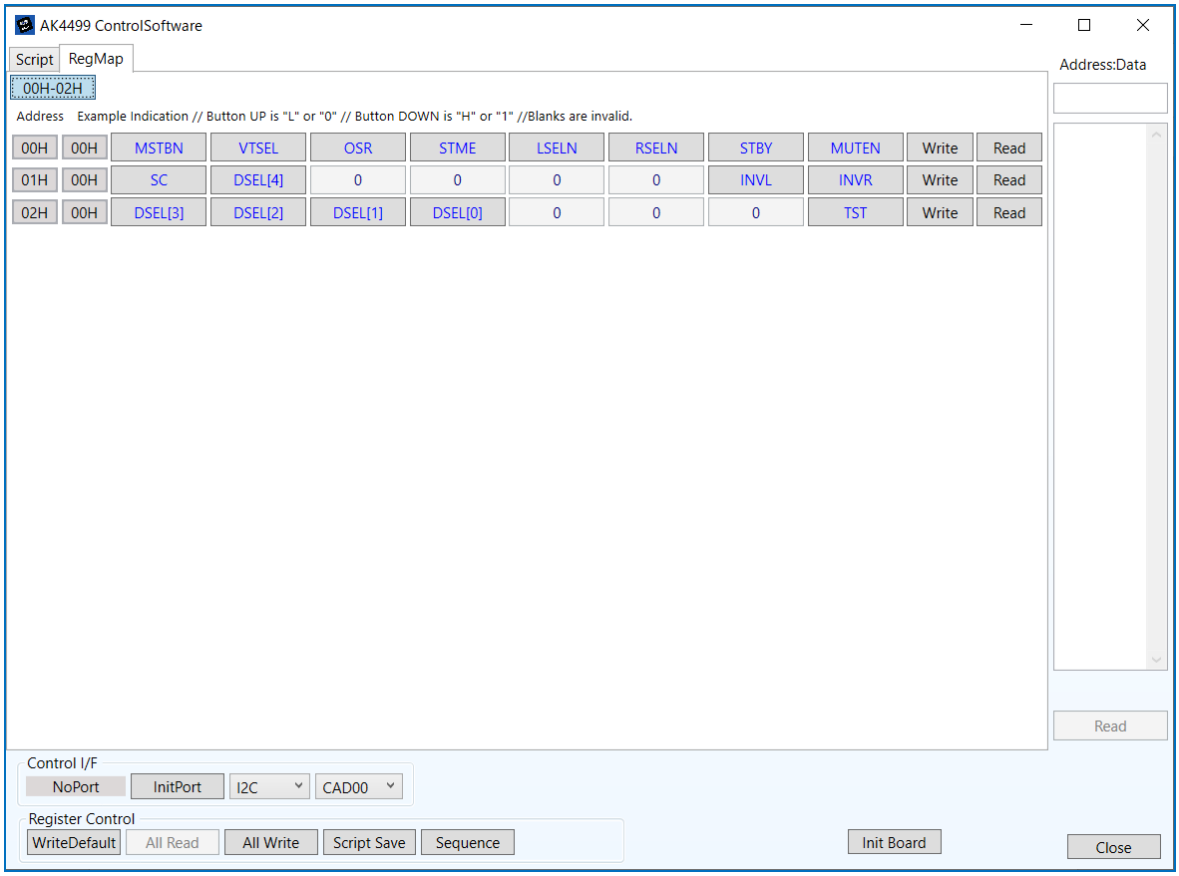


Figure 14-1. RegMap Window

[Write] button: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

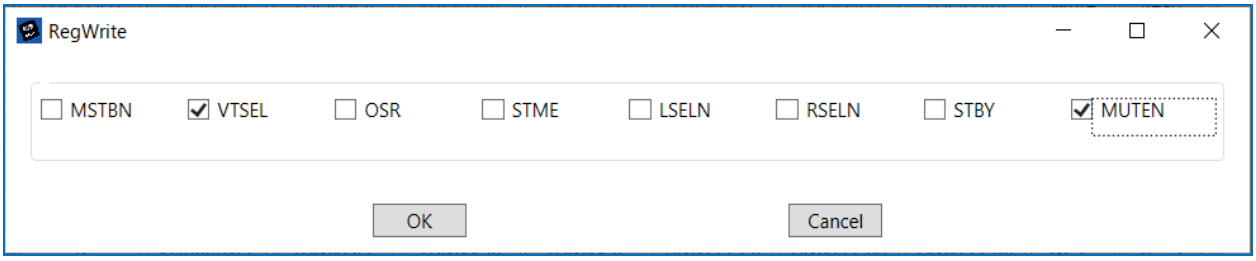


Figure 14-2. Register Set Window

[Read] button: Data Read (Only in I²C-bus Control Mode)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.
Button Down indicates “1” and the bit name is shown in red (when read only the bit name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

2. [Script] Tab : Script Function

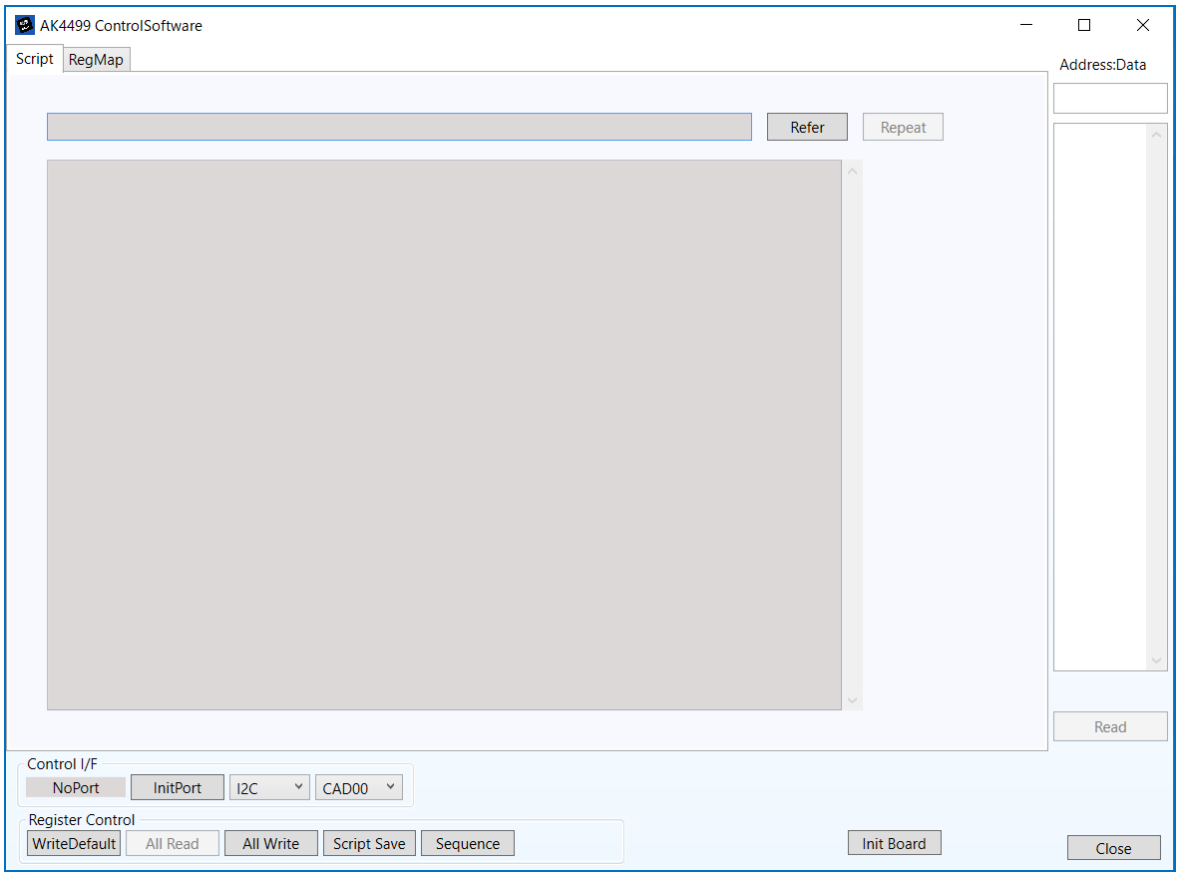


Figure 15. Window of [Script]

[Refer] : Select a script file. The script written on the file will be executed automatically.
[Repeat] : The selected script file will be executed once again.

■ Dialog Box

1. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

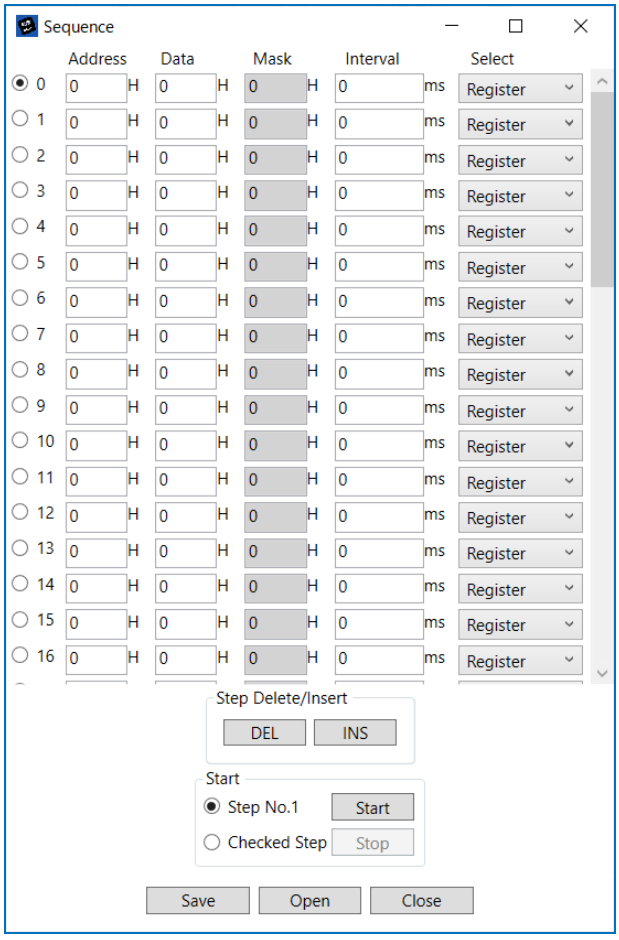


Figure 16. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

   Use [Select] pull-down box to choose commands.
   Corresponding input boxes will be valid.

<Combo Box>

- No_use: Not using this address
- Register: Register write
- Reg(Mask): Register write (Masked)
- Interval: Take an interval
- Stop: Pause the sequence
- End: End the sequence

2. Input Sequence

[Address]: Data Address
[Data]: Write Data
[Mask]: Mask
This value “ANDed” with the write data becomes the input data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

[Start] button : Execute the sequence.
[Stop] button : Pause the sequence.
[Save] button : Save sequence settings as a file. The file name is “*.aks”.
[Open] button : Open a sequence setting file “*.aks”.
[Close] button : Close the dialog box and finishes the process.

Start Sequence: [Start] Functions

[Step No.1] check box : Start at number “0” in the sequence.
[Checked Step] check box : Start from checked number in the sequence.

Revision History

Date (y/m/d)	Manual Revision	Board Revision	Reason	Page	Contents
22/06/01	KM136300	0	First Edition	-	-

IMPORTANT NOTICE

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Rev.1

1. Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision APX555 audio analyzer (APX555)
- MCLK : 22.5792MHz
- BICK : 64fs
- fs : 44.1kHz
- Bit : 24bit
- Power Supply for AK4499EX
  : AVDD=5.0V, TVDD=3.3V, DVDD=1.8V
  VDDL/R=5.0V, VREFHL/R=5.0V
- Pass : DIR → AK4191 → AK4499EX → Cannon Connector
- Interface : Internal DIR (44.1 kHz)
- Temperature : Room Temperature
- Operational Amplifiers : OPA1612

fs=44.1kHz : 0dBr= 8.960Vrms / 8.884Vrms (GC3-0 bit=0110, VTSEL bit=1)
OSR128 mode (OSR bit="H") : Operation rate=OSR128=5.6448MHz, Modulator Data=7bit data mode

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD	1kHz, 0dB	20kHz LPF	125.2 dB	/	124.1 dB
		40kHz LPF	125.2 dB	/	124.1 dB
		80kHz LPF	125.2 dB	/	124.1 dB
DR	1kHz, -60dB	20kHz LPF	129.4 dB	/	129.4 dB
		40kHz LPF	126.8 dB	/	126.6 dB
		80kHz LPF	122.8 dB	/	122.6 dB
		20kHz LPF A-weighted	132.5 dB	/	132.5 dB
S/N	"0" data	20kHz LPF	132.6 dB	/	132.6 dB
		40kHz LPF	129.8 dB	/	129.7 dB
		80kHz LPF	127.3 dB	/	127.3 dB
		20kHz LPF A-weighted	135.0 dB	/	135.0 dB

OSR256 mode (OSR bit="L") : Operation rate=OSR256=11.2896MHz, Modulator Data=7bit data mode

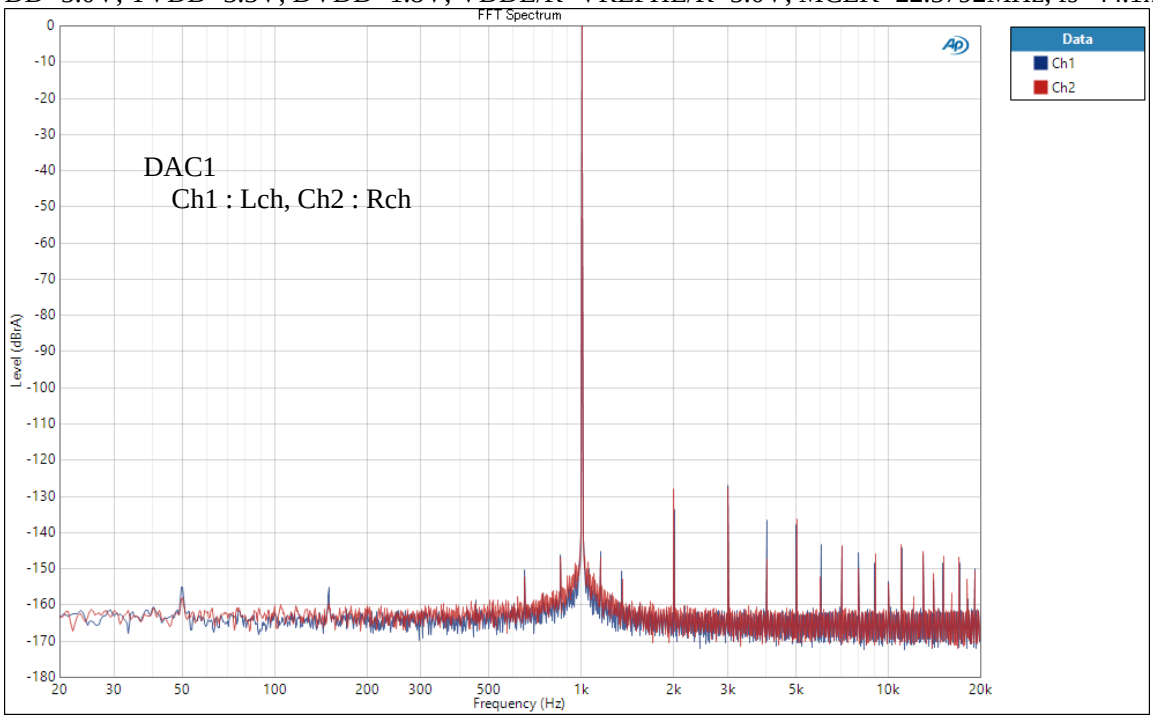
Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD	1kHz, 0dB	20kHz LPF	121.3 dB	/	118.2 dB
		40kHz LPF	121.3 dB	/	118.2 dB
		80kHz LPF	121.3 dB	/	118.2 dB
DR	1kHz, -60dB	20kHz LPF	128.4 dB	/	128.4 dB
		40kHz LPF	126.2 dB	/	126.0 dB
		80kHz LPF	121.2 dB	/	121.1 dB
		20kHz LPF A-weighted	129.5 dB	/	129.5 dB
S/N	"0" data	20kHz LPF	132.1 dB	/	132.1 dB
		40kHz LPF	129.3 dB	/	129.2 dB
		80kHz LPF	126.8 dB	/	126.7 dB
		20kHz LPF A-weighted	134.4 dB	/	134.5 dB

[Plots]

OSR128 Mode, fs = 44.1 kHz

AK4499EX FFT (0dBFS Input)

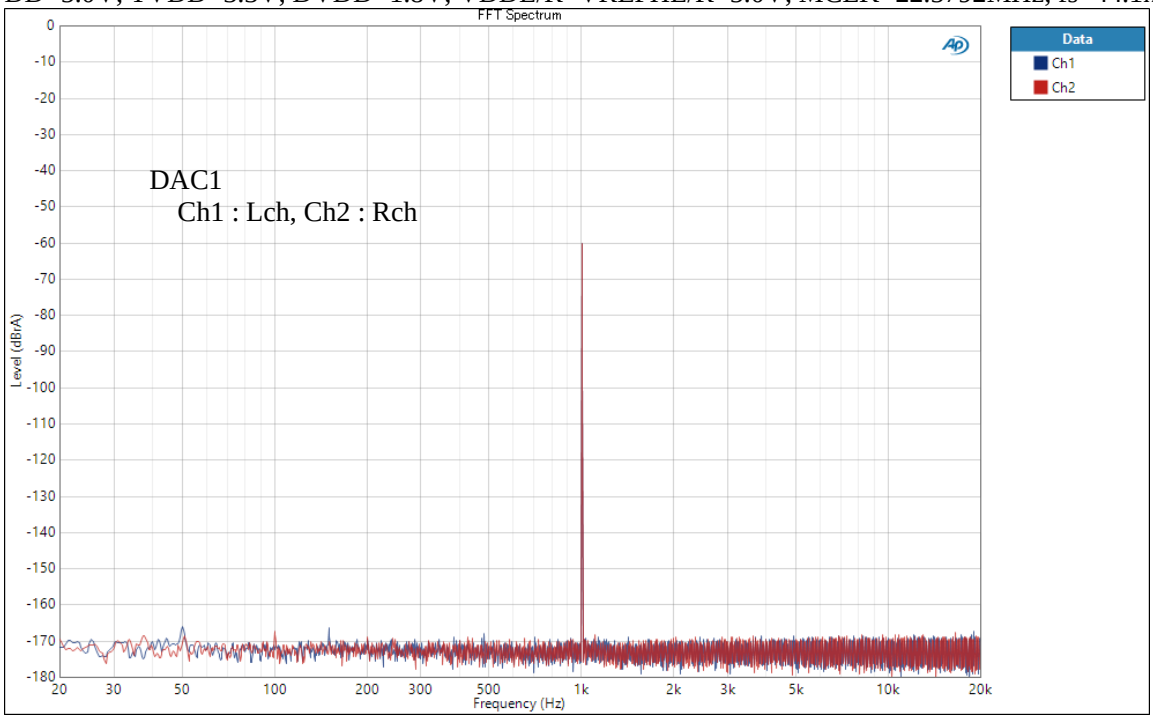
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz



Plot Figure A-1. FFT (0dBFS Input)

AK4499EX FFT (-60dBFS Input)

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz

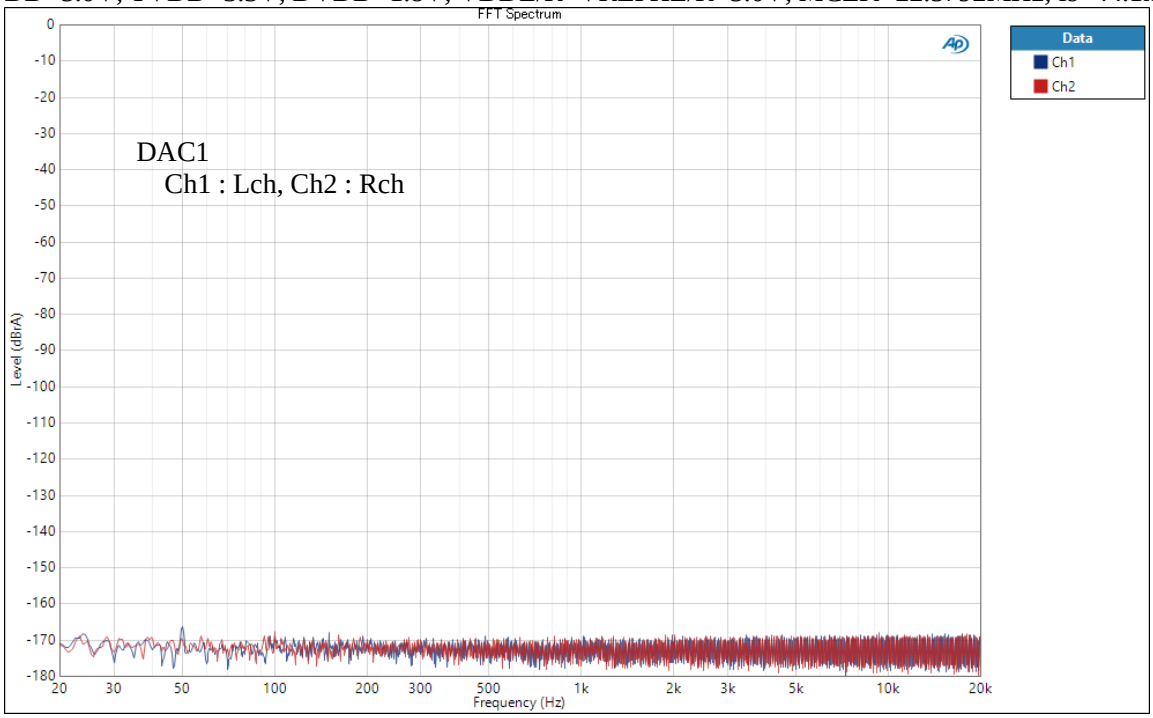


Plot Figure A-2. FFT (-60dBFS Input)

OSR128 Mode, fs = 44.1 kHz

AK4499EX FFT (-240dBFS Input)

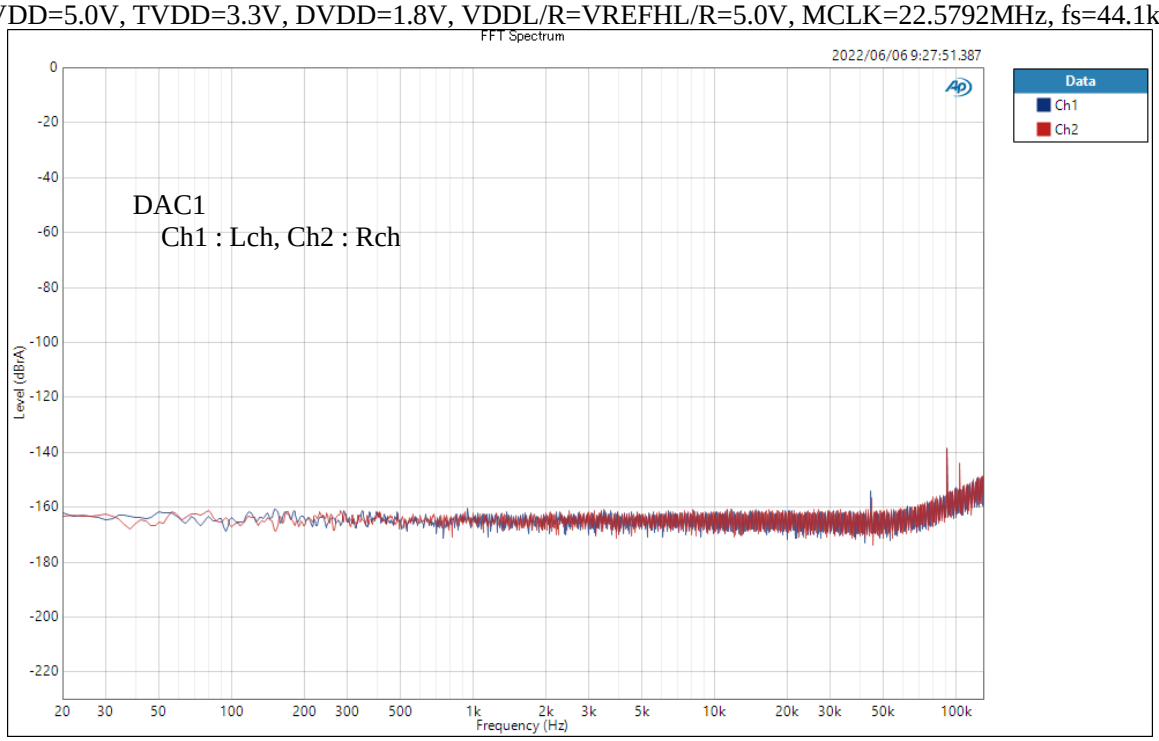
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz



Plot Figure A-3. FFT (-240dBFS Input)

AK4499EX Out of Band Noise (-240dBFS Input)

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz



Plot Figure A-4. Out of Band Noise (-240dBFS Input)

OSR128 Mode, fs = 44.1 kHz

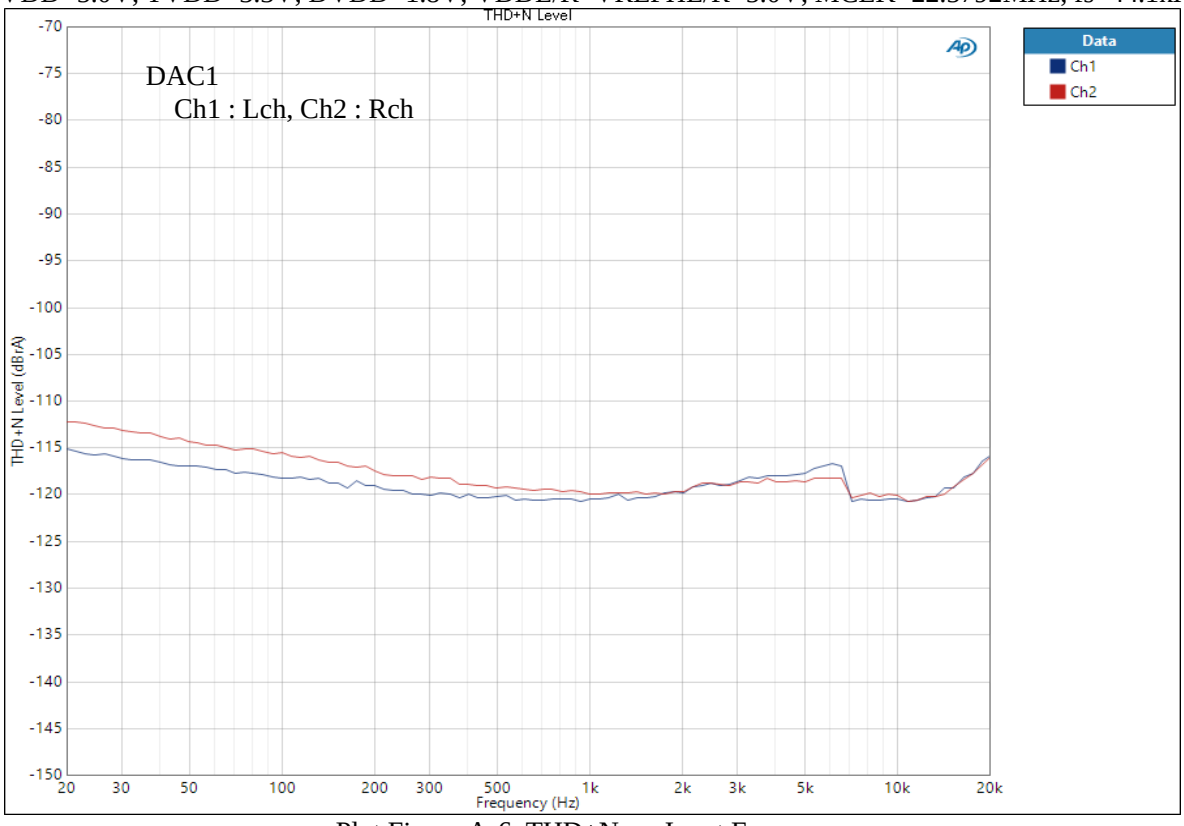
AK4499EX THD+N vs. Input Level

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz

Plot Figure A-5. THD+N vs. Input Level

AK4499EX THD+N vs. Input Frequency

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz

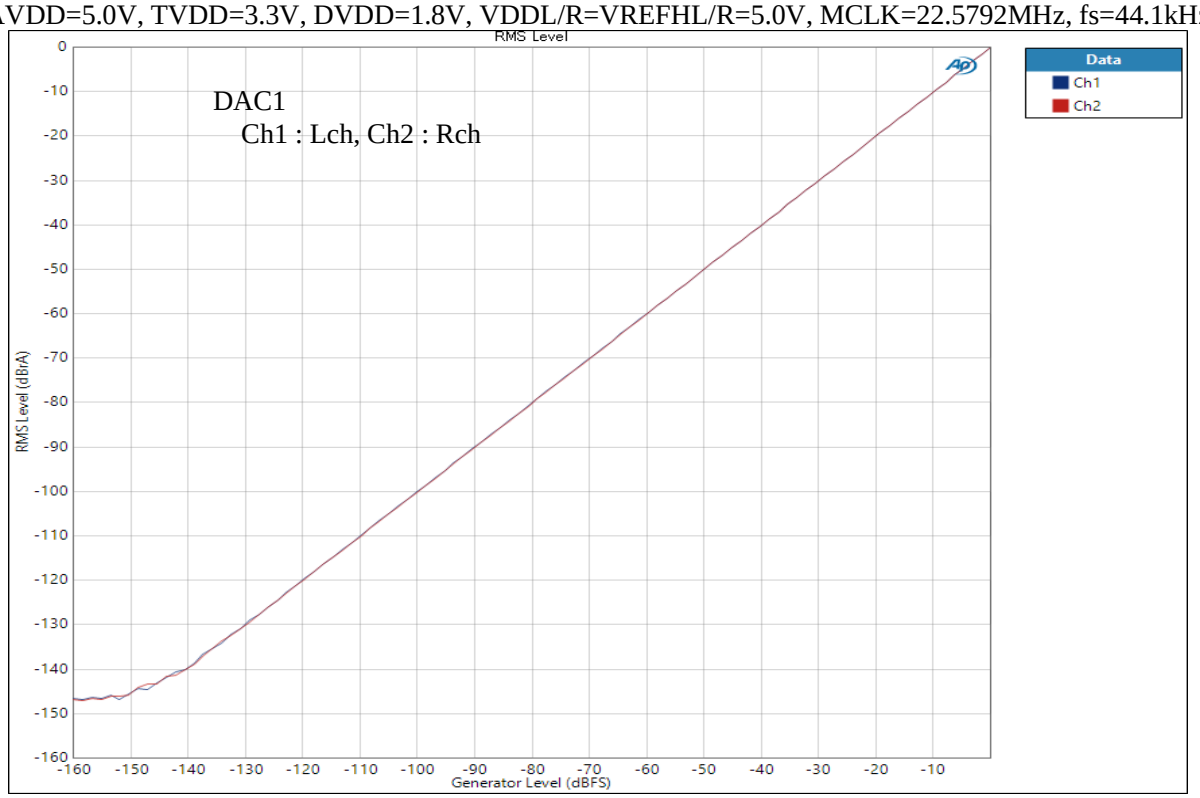


Plot Figure A-6. THD+N vs. Input Frequency

OSR128 Mode, fs = 44.1 kHz

AK4499EX Linearity

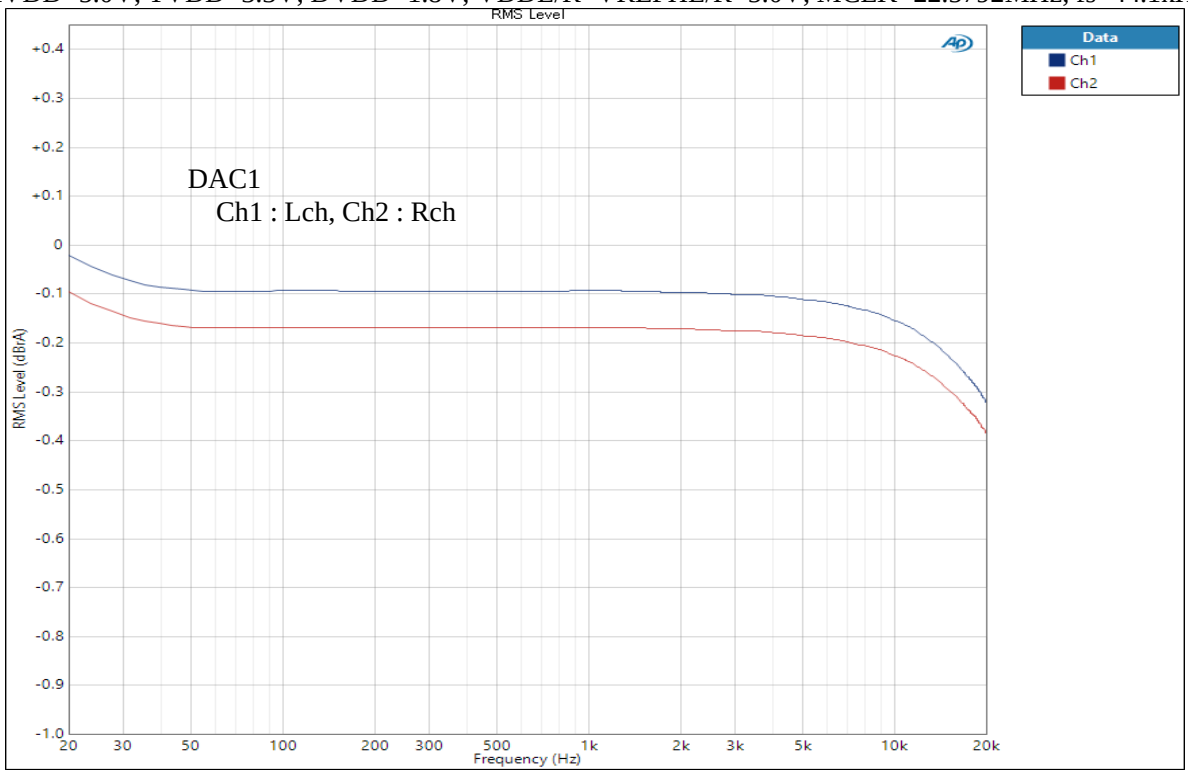
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz



Plot Figure A-7. Linearity

AK4499EX Frequency Response

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz

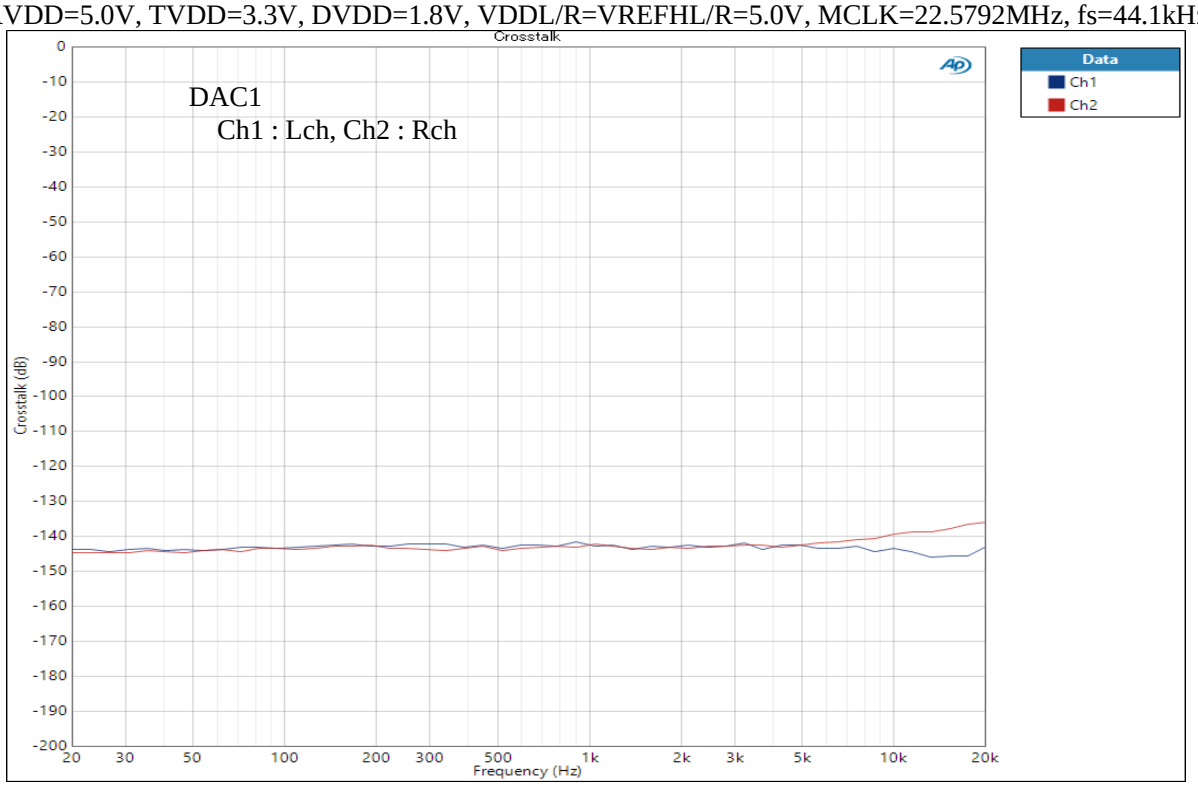


Plot Figure A-8. Frequency Response

OSR128 Mode, fs = 44.1 kHz

AK4499EX Crosstalk

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=44.1kHz

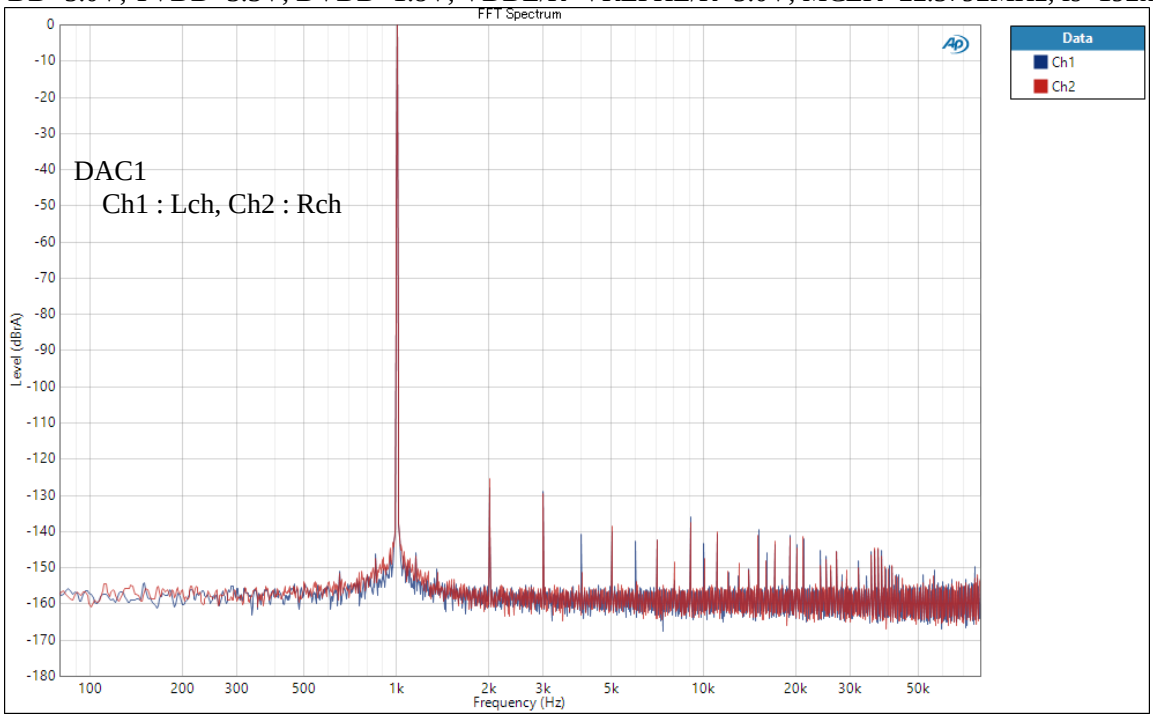


Plot Figure A-9. Crosstalk

OSR128 Mode, fs = 192 kHz

AK4499EX FFT (0dBFS Input)

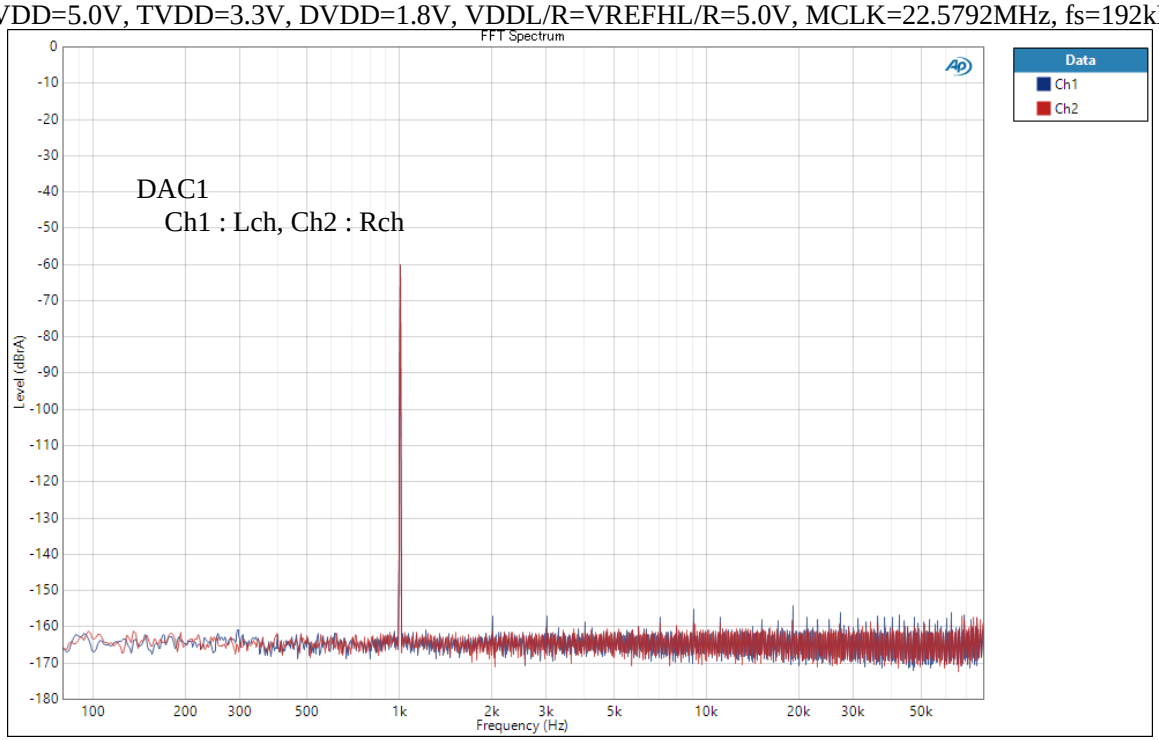
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz



Plot Figure B-1. FFT (0dBFS Input)

AK4499EX FFT (-60dBFS Input)

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz

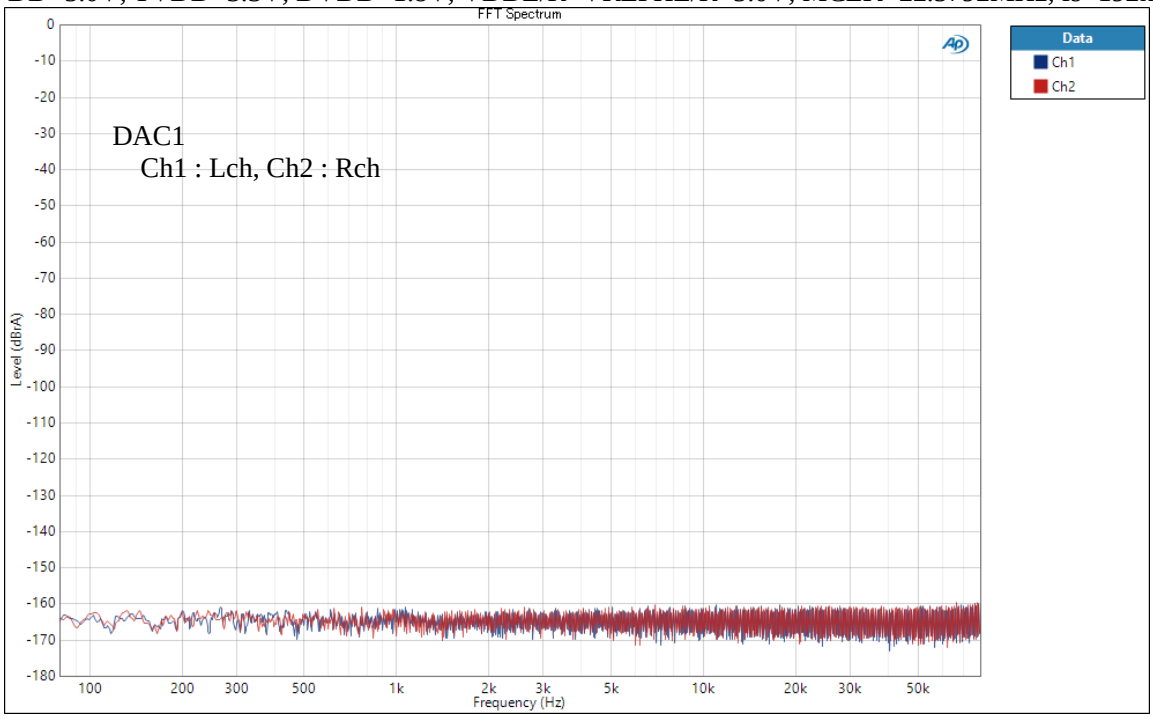


Plot Figure B-2. FFT (-60dBFS Input)

OSR128 Mode, fs = 192 kHz

AK4499EX FFT (-240dBFS Input)

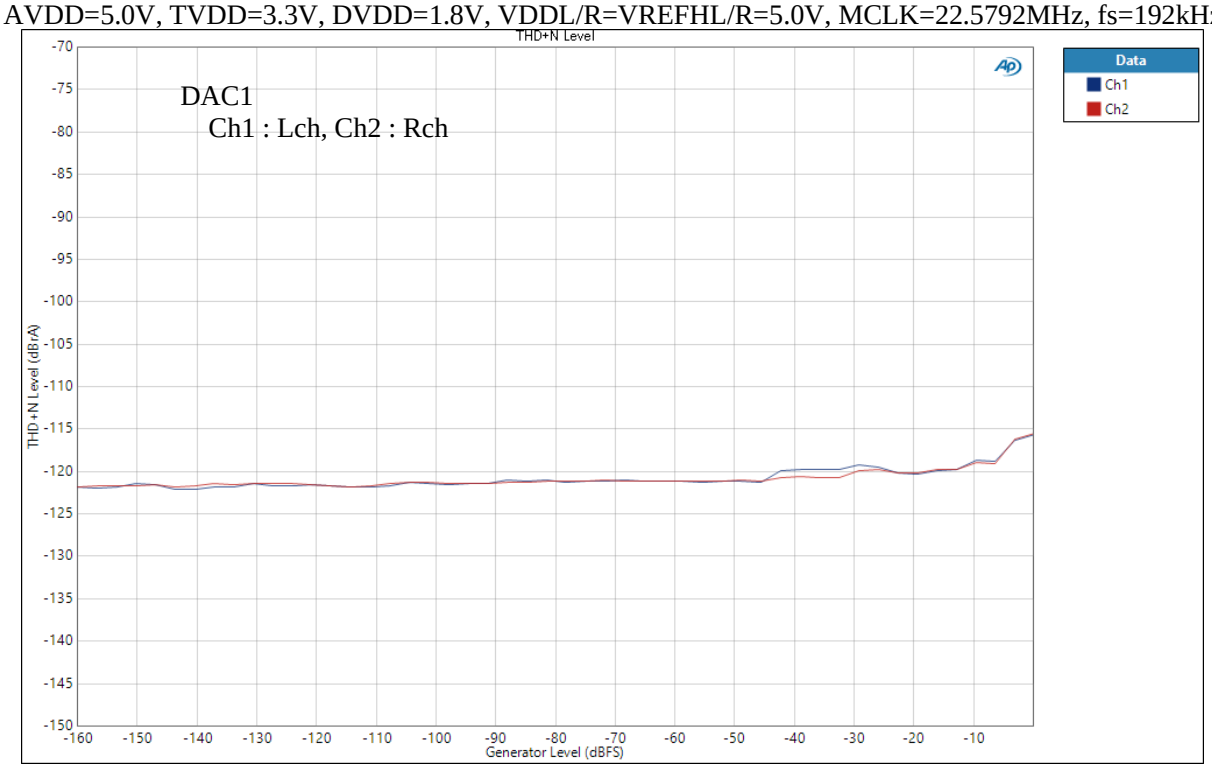
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz



Plot Figure B-3. FFT (-240dBFS Input)

AK4499EX THD+N vs. Input Level

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz

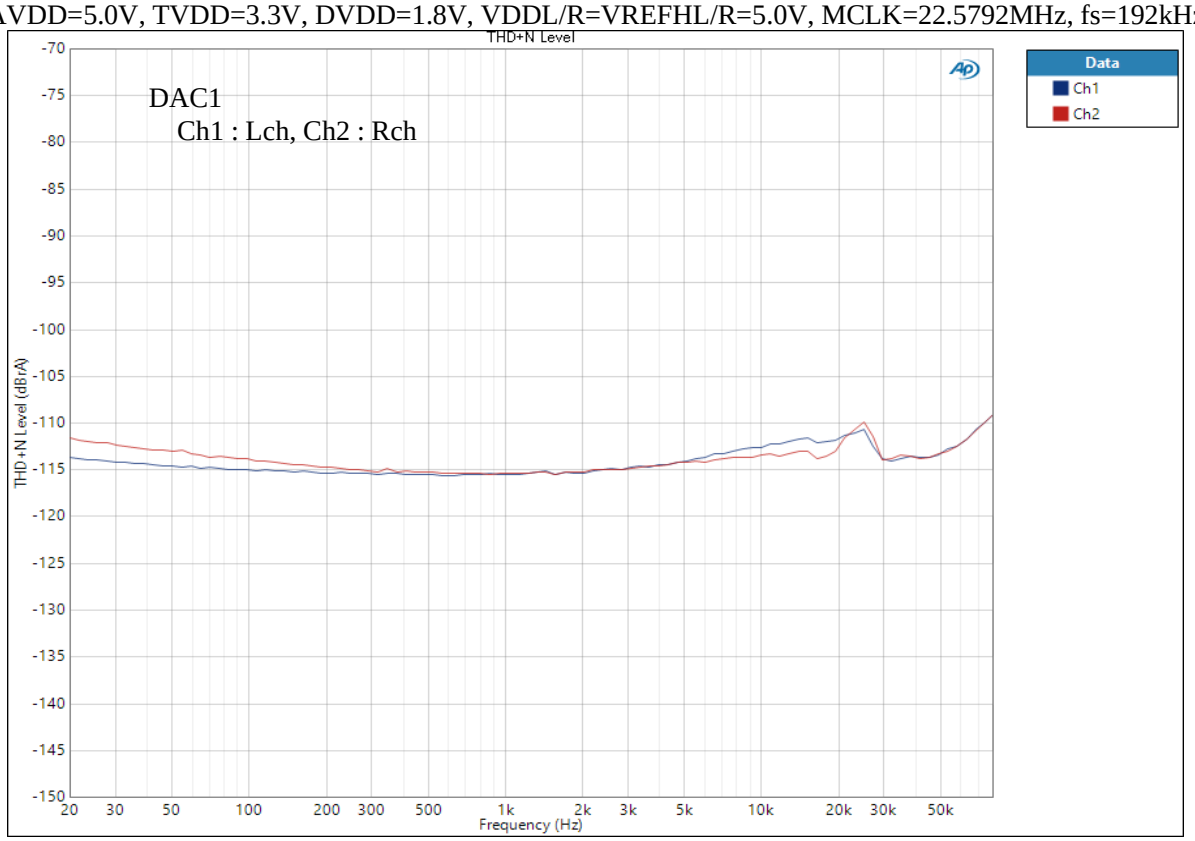


Plot Figure B-4. THD+N vs. Input Level

OSR128 Mode, fs = 192 kHz

AK4499EX THD+N vs. Input Frequency

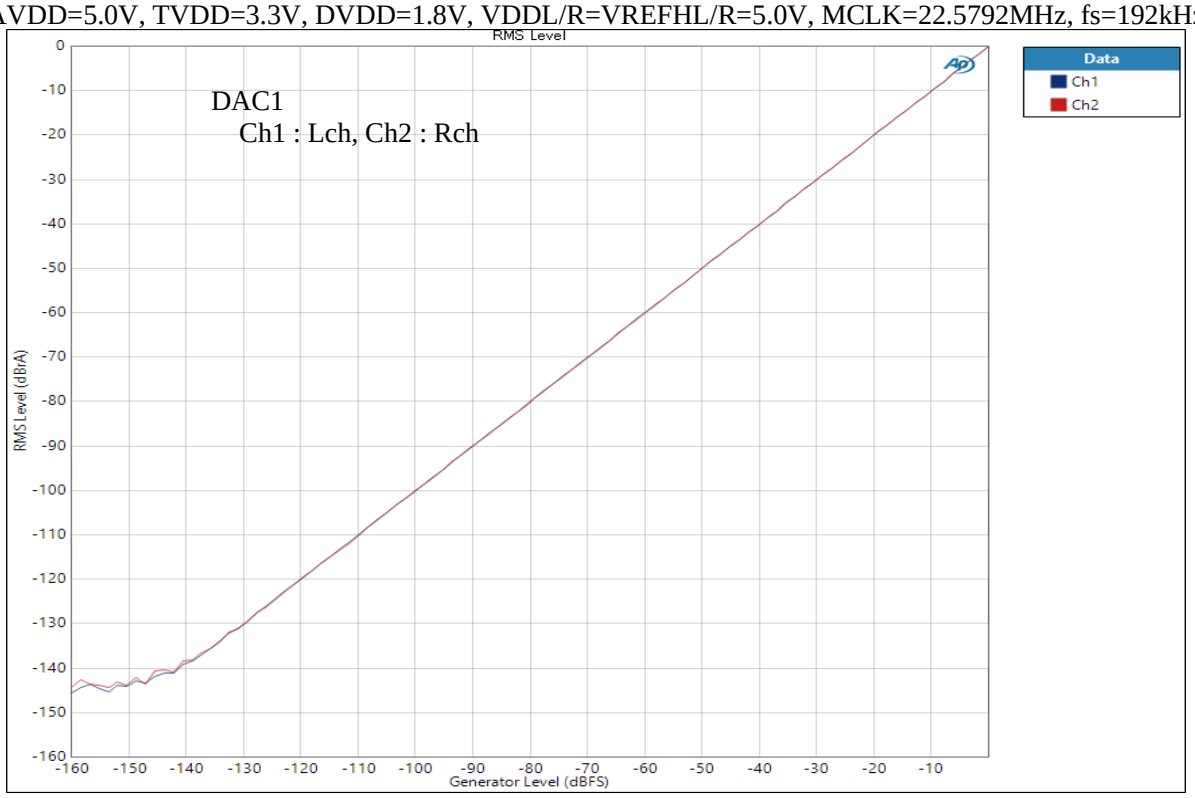
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz



Plot Figure B-5. THD+N vs. Input Frequency

AK4499EX Linearity

AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz

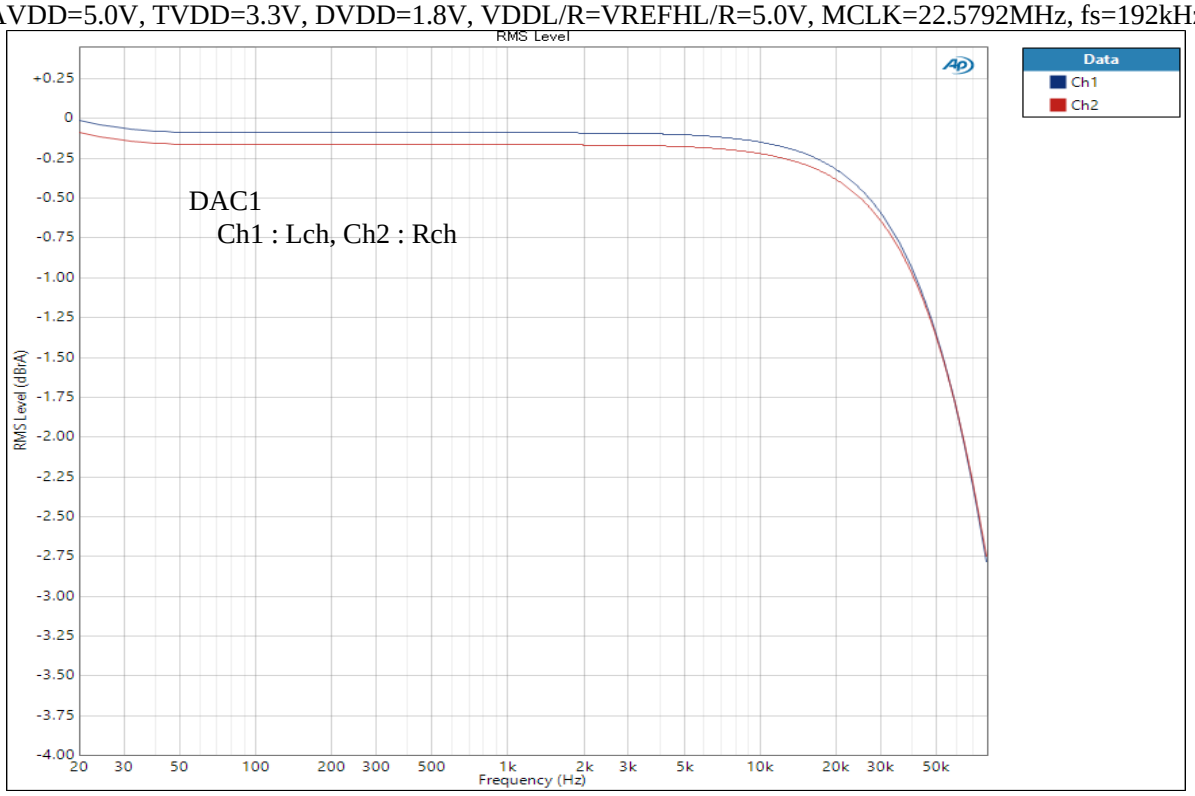


Plot Figure B-6. Linearity

OSR128 Mode, fs = 192kHz

AK4499EX Frequency Response

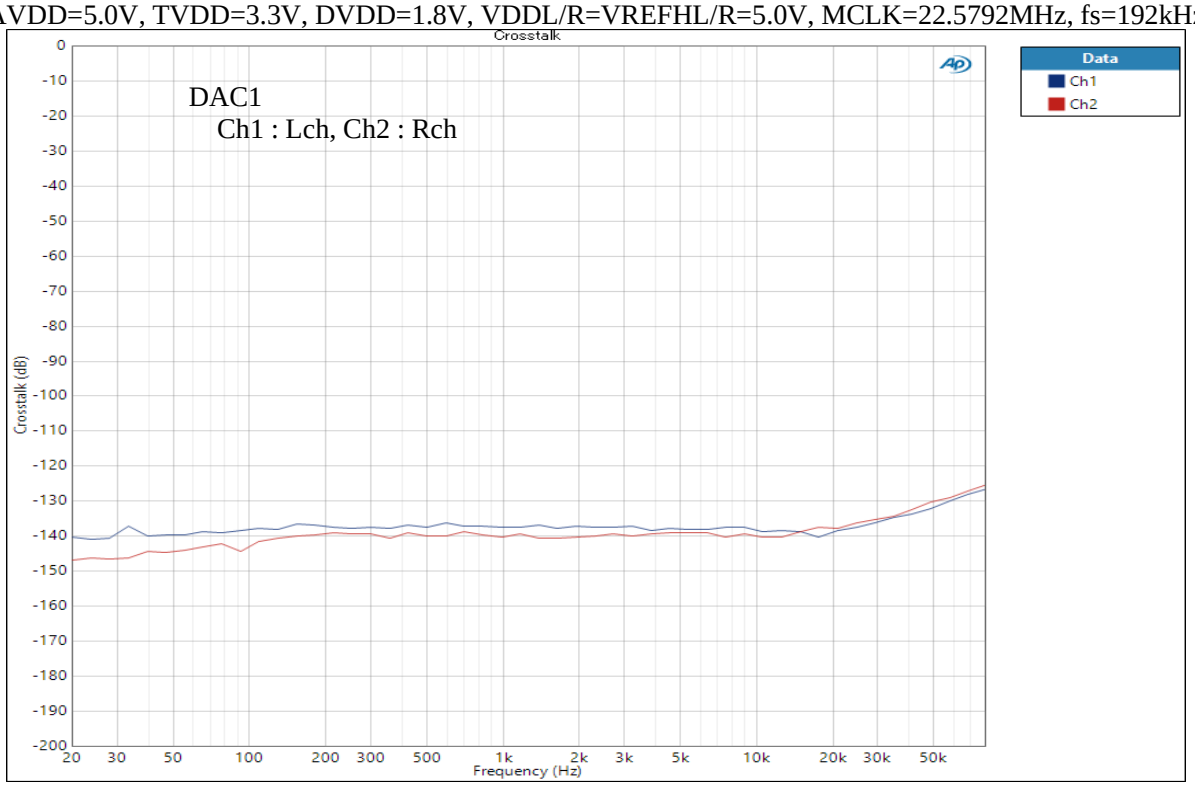
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz



Plot Figure B-7. Frequency Response

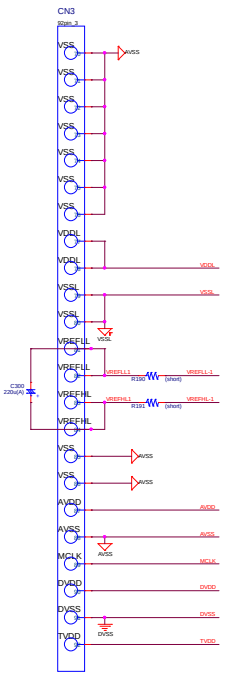
AK4499EX Crosstalk

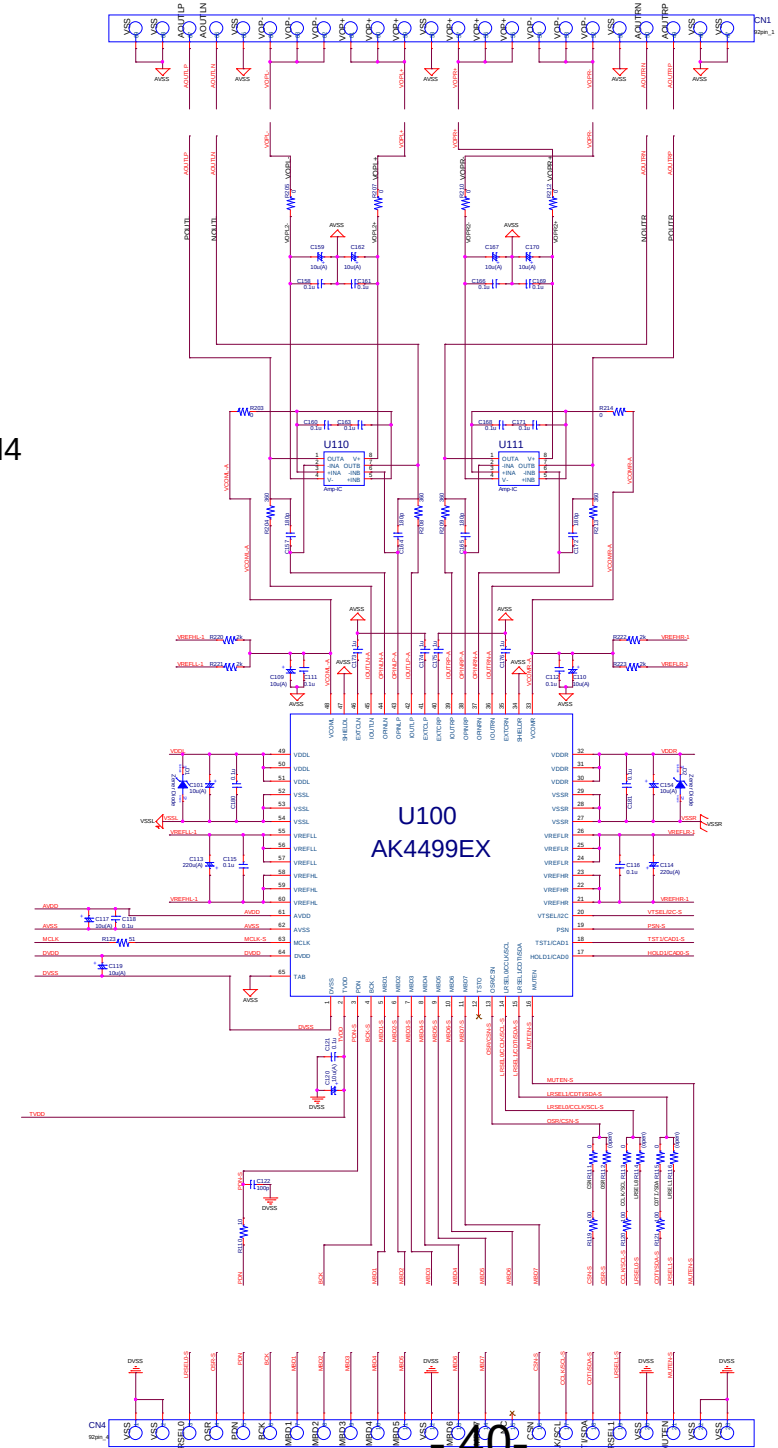
AVDD=5.0V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5.0V, MCLK=22.5792MHz, fs=192kHz

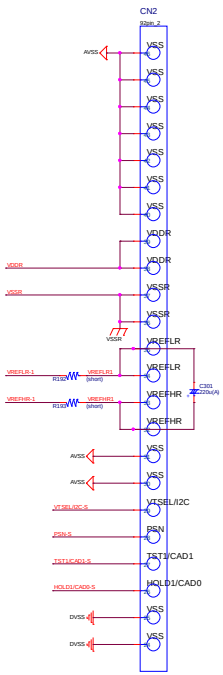


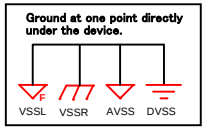
Plot Figure B-8. Crosstalk

CN1, CN2, CN3, CN4
OY-003 (23pin)









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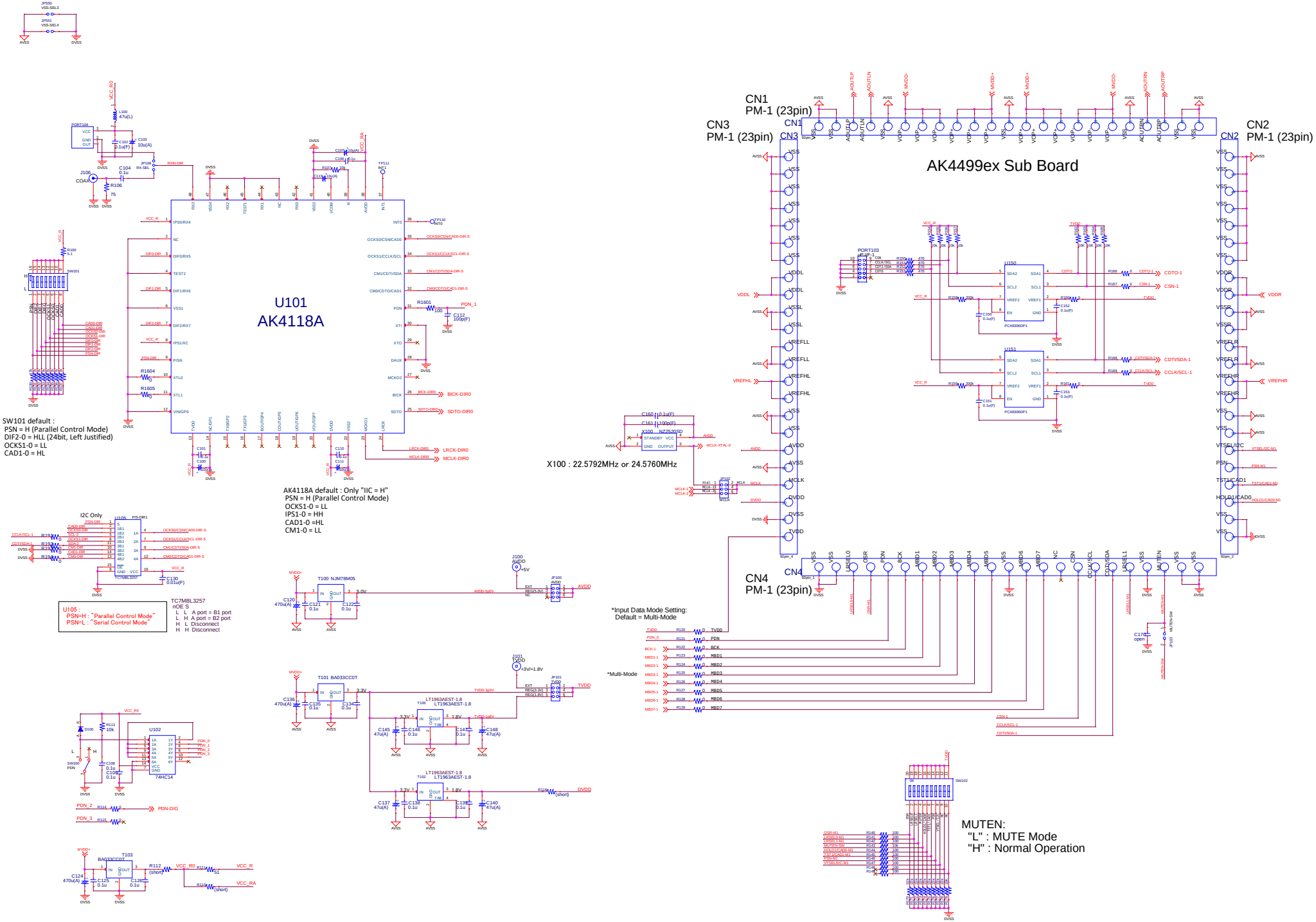
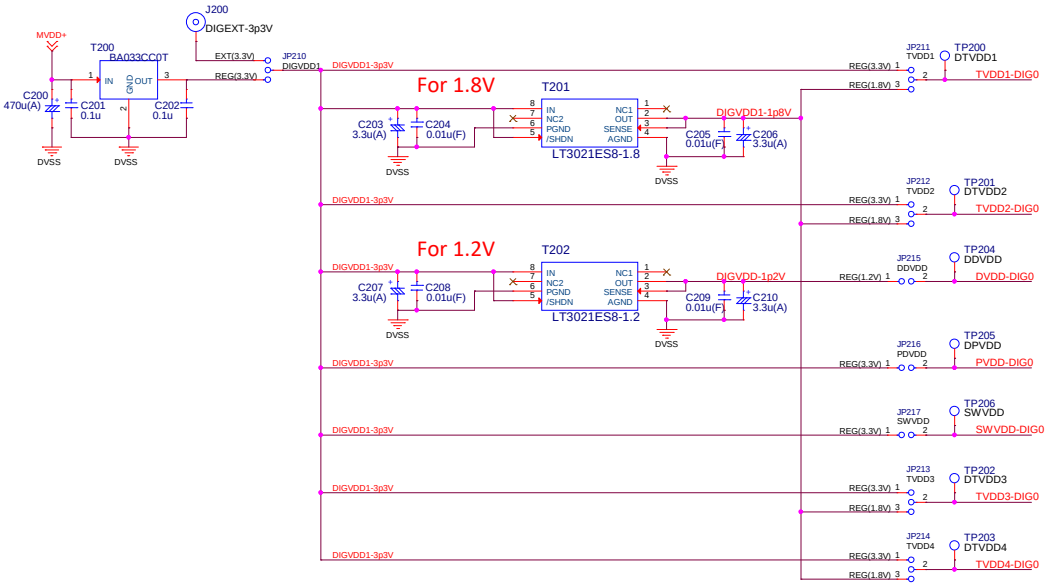
Size A1	Document Number AK4499EX	Rev 0
Date: Wednesday, June 08, 2022	Sheet 1 of 1	

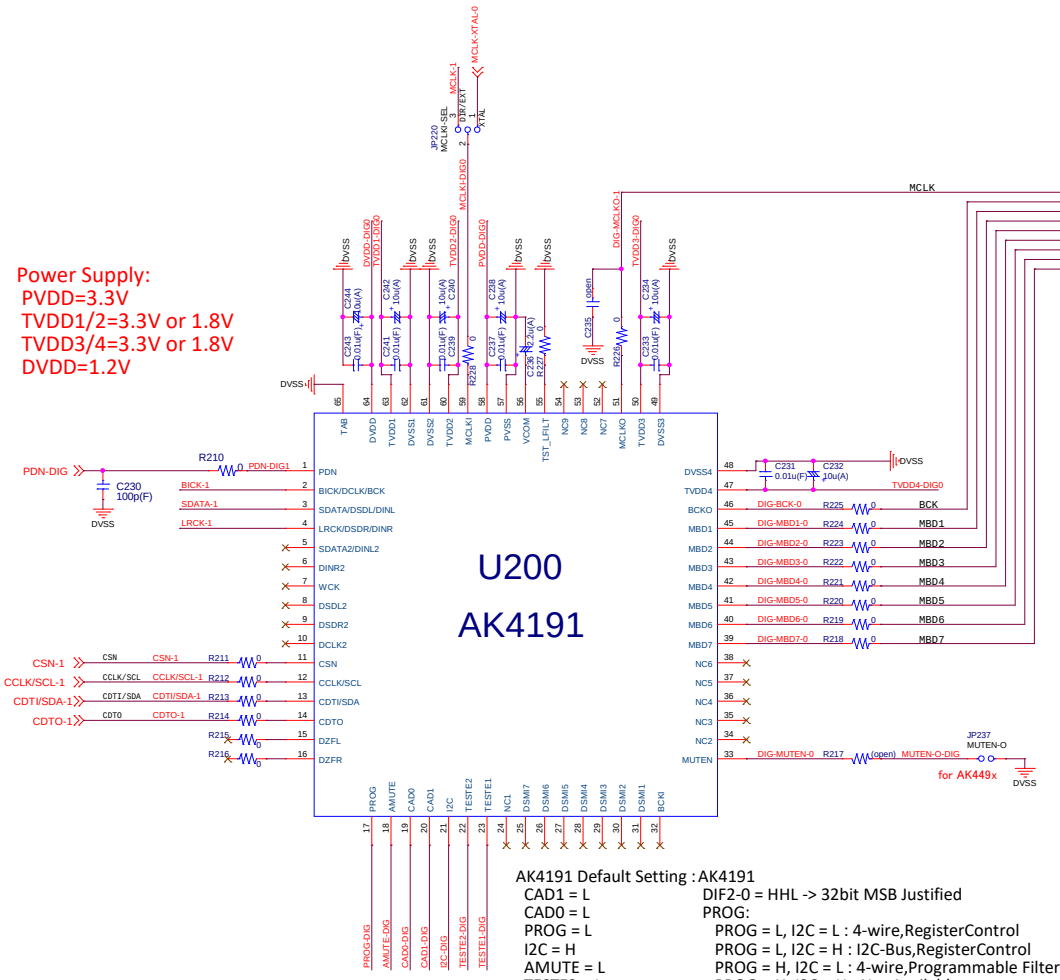


Title	AKD4499EX-A-MAIN	
Size: A1	Document Number: Under the Sub-board	Rev: 0
Date: Wednesday, June 08, 2022	Sheet 1 of 4	

AK4191 Digital-IC Block



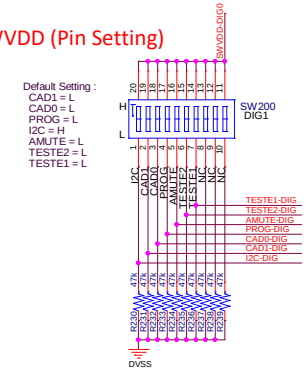
Power Supply:
PVDD=3.3V
TVDD1/2=3.3V or 1.8V
TVDD3/4=3.3V or 1.8V
DVDD=1.2V

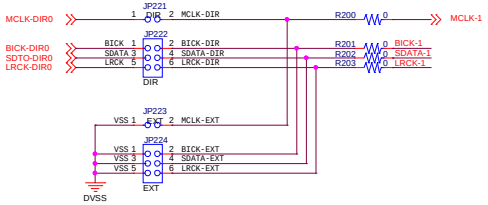


AK4191 Default Setting : AK4191
CAD1 = L
CAD0 = L
PROG = L
I2C = H
AMUTE = L
TESTE2 = L
TESTE1 = L

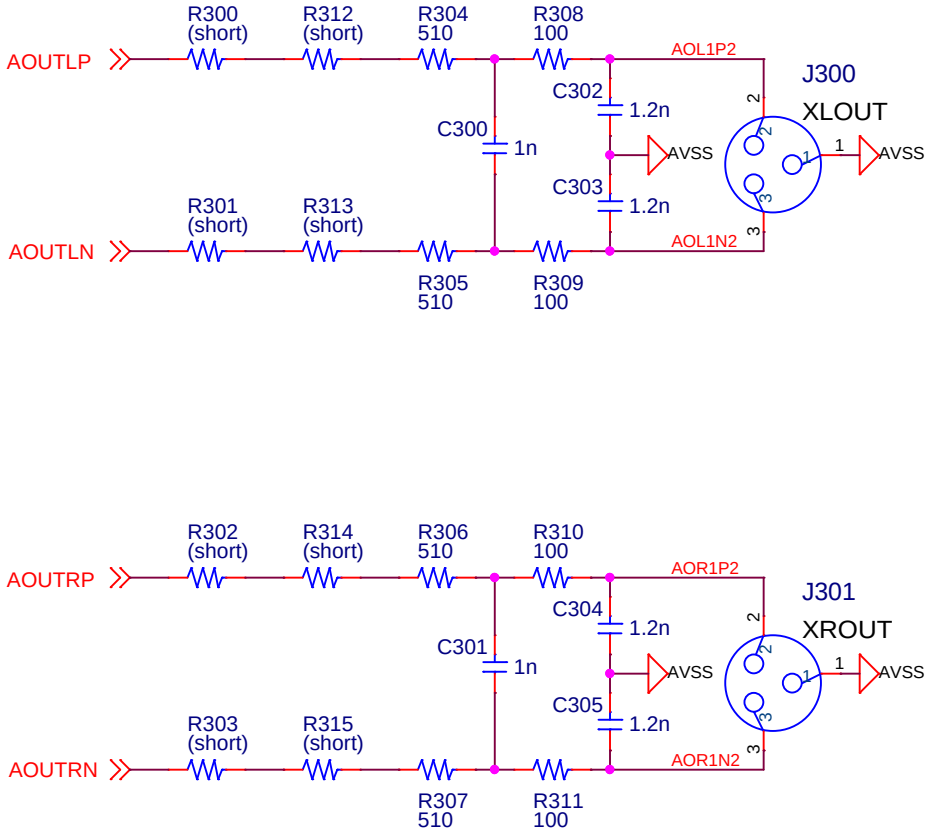
DIF2-0 = HHL -> 32bit MSB Justified
PROG:
PROG = L, I2C = L : 4-wire,RegisterControl
PROG = L, I2C = H : I2C-Bus,RegisterControl
PROG = H, I2C = L : 4-wire,Programmable Filter
PROG = H, I2C = H : Not Available
MUTEN: Output Signal
MUTEN="L" : Mute cycle
MUTEN="H" : Mute releases

For SWVDD (Pin Setting)





Title	AKD4499EX-A-MAIN
Size	A2
Document Number	AK4191
Rev	0
Date:	Wednesday, June 08, 2022
Sheet	2 of 4



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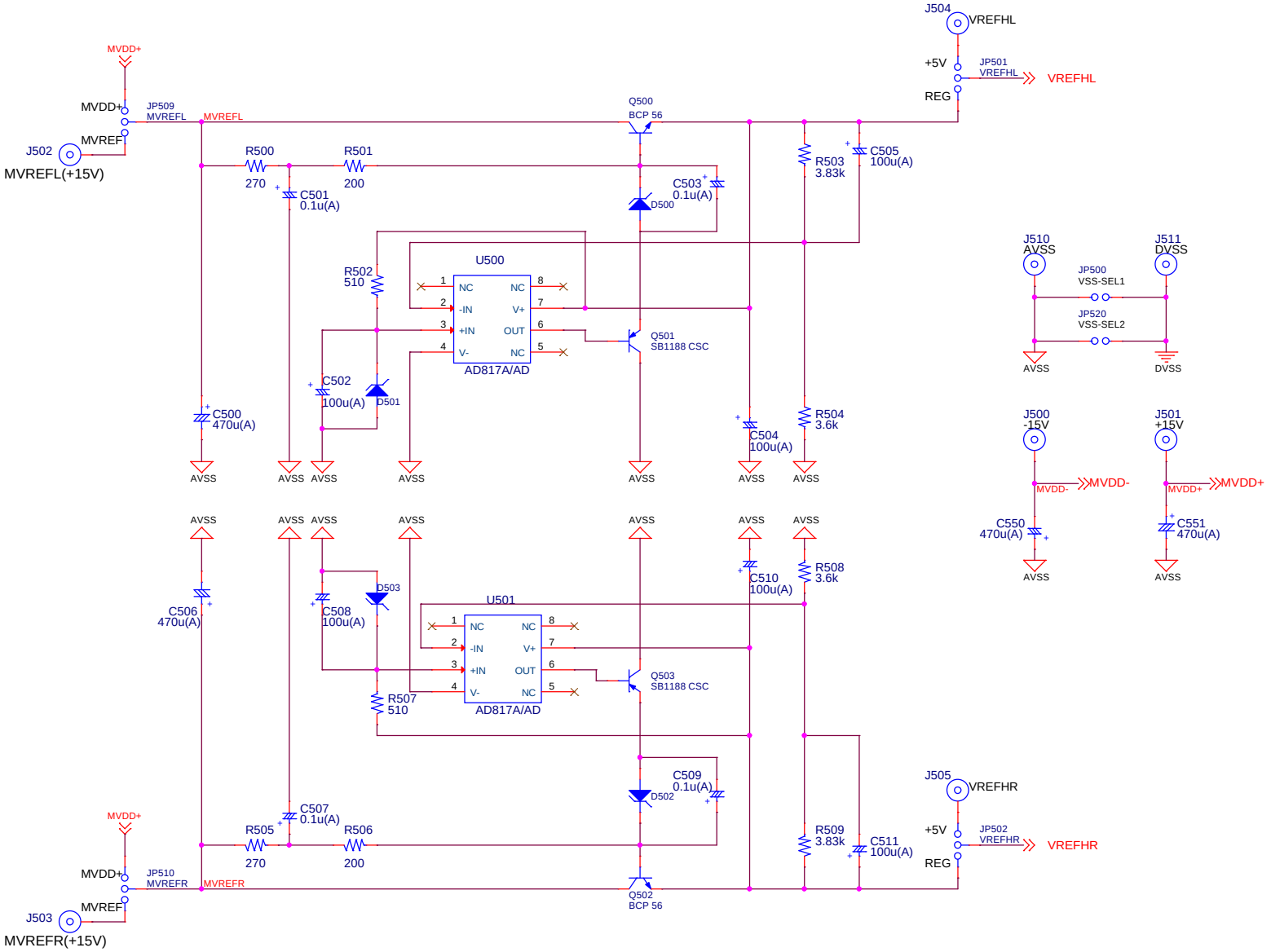
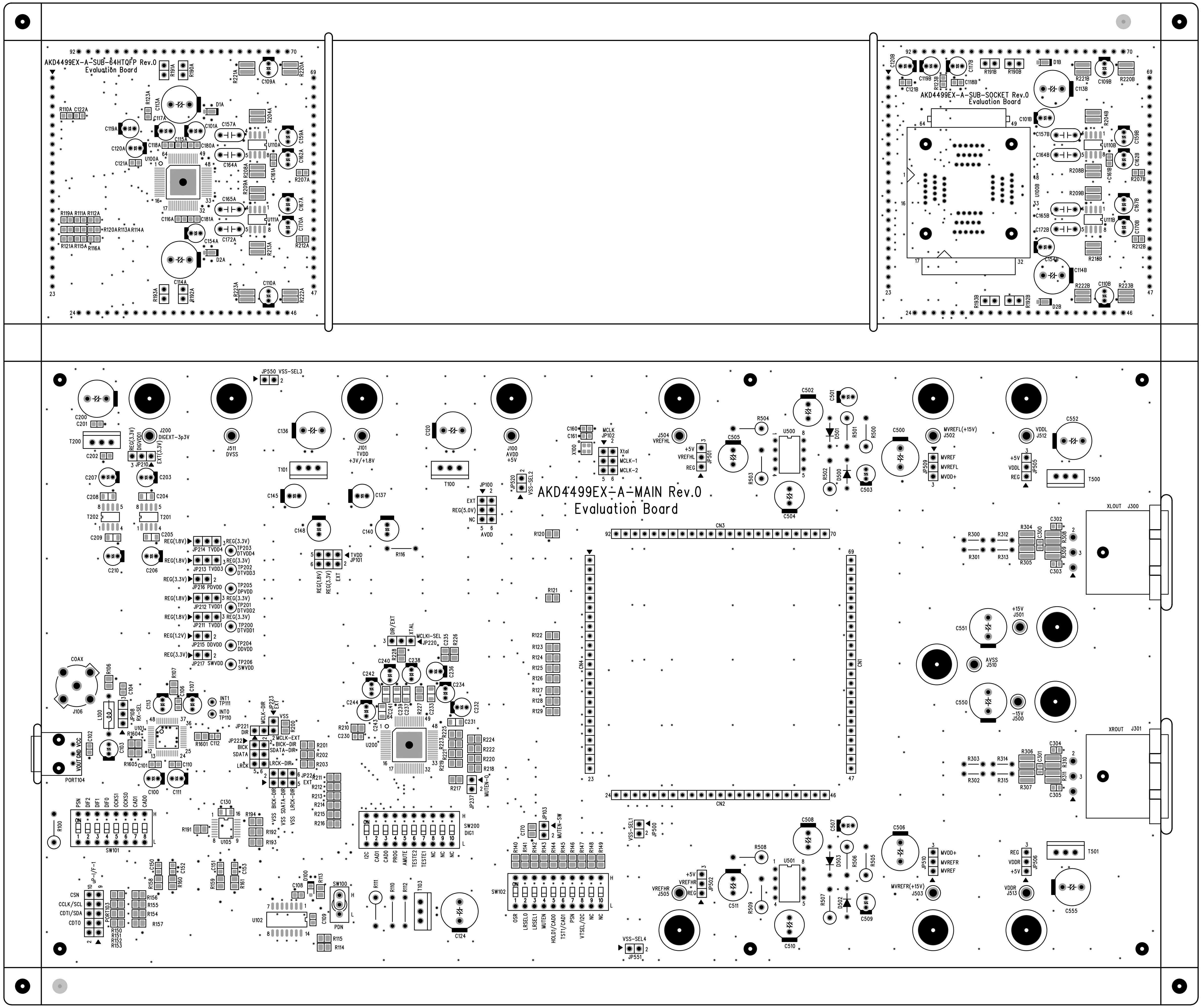
Size A4	Document Number External LPF2 Analog Output	Rev 0
Date: Wednesday, June 08, 2022	Sheet 3 of 4	



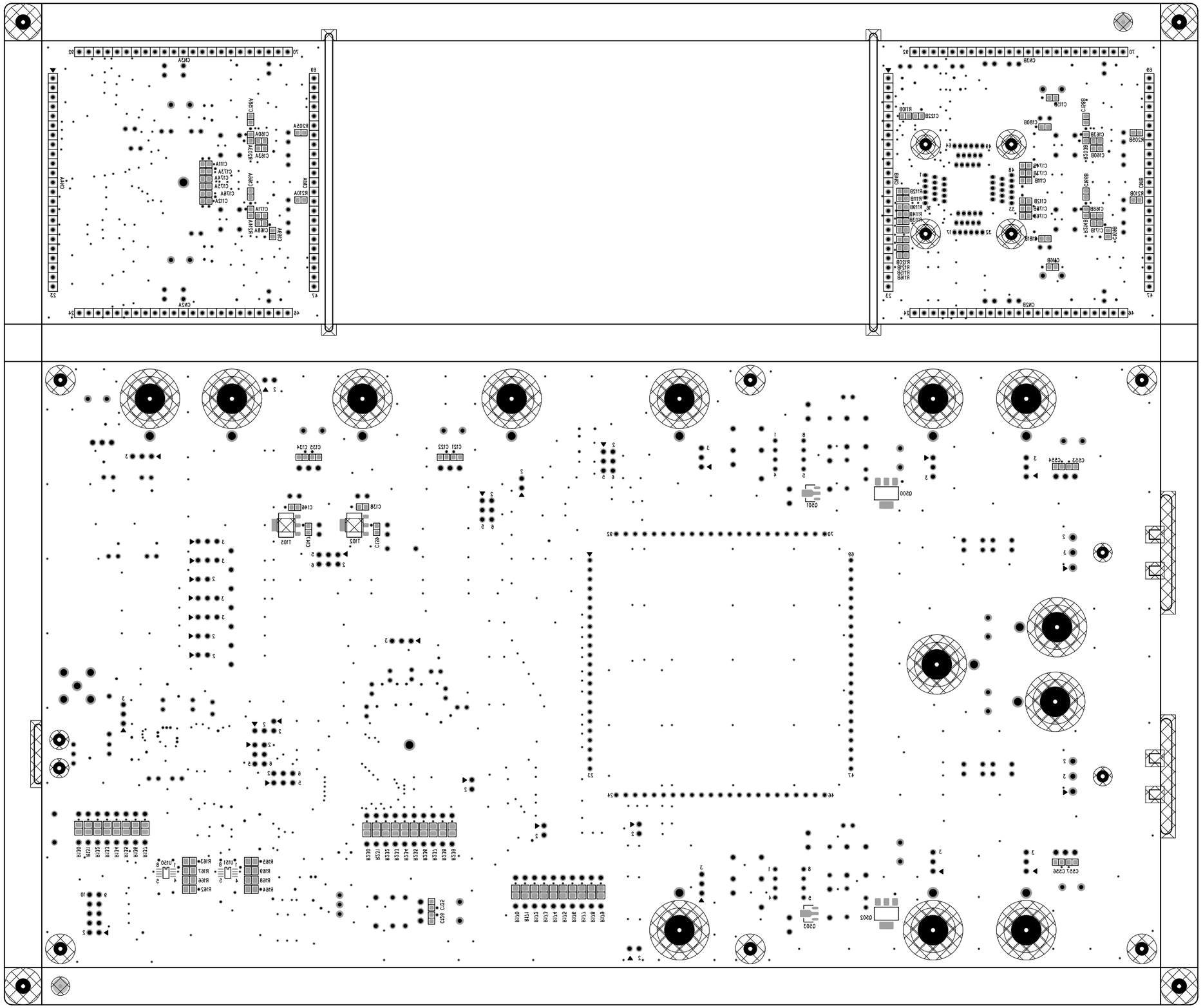
Title	AKD4499EX-A-MAIN	
Size A3	Document Number Power Supply Unit	Rev 0
Date: Wednesday, June 08, 2022	Sheet 4 of 4	

AKD4499EX-A_Rev0

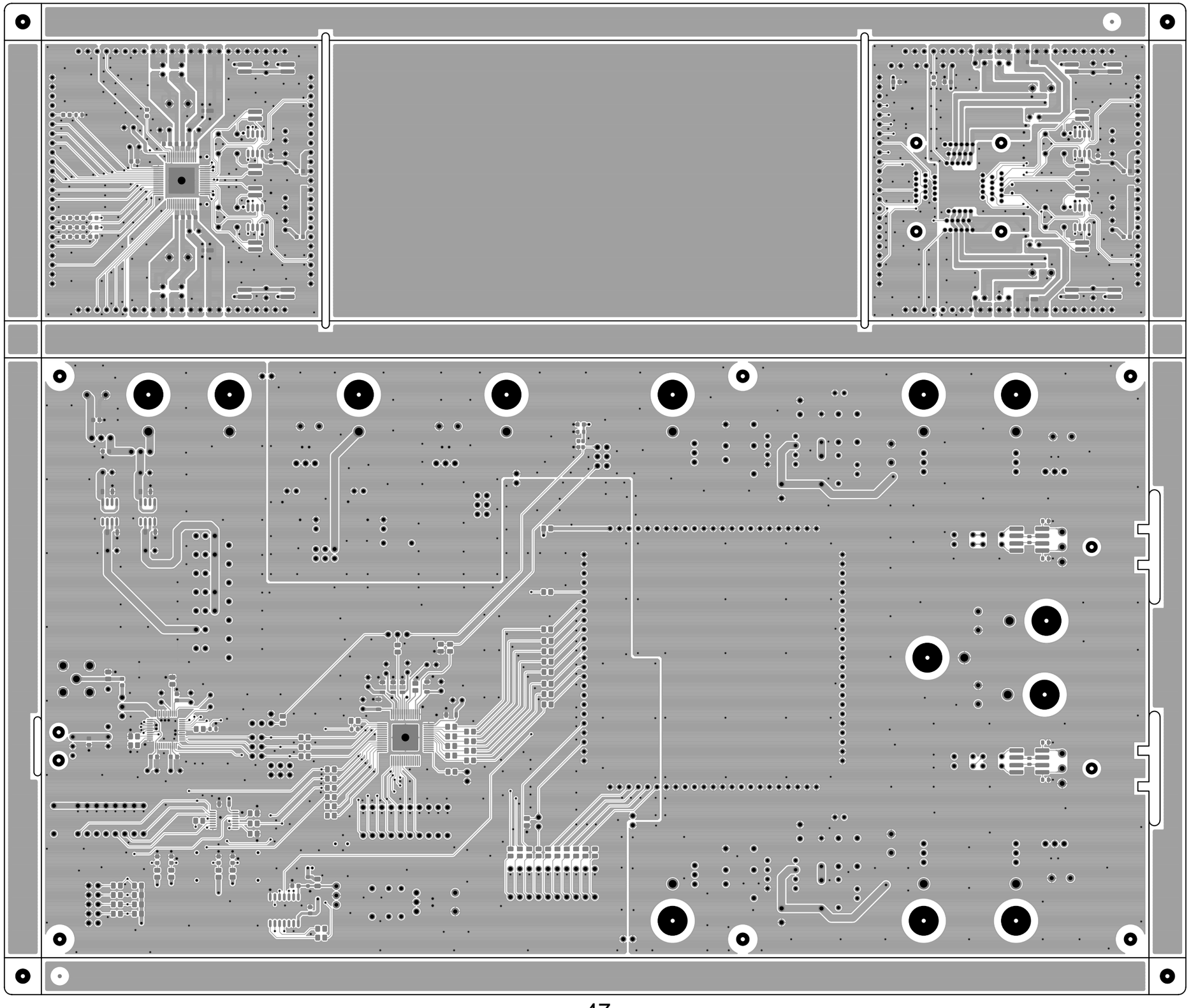
部品面シルク図　(部品面透視図)



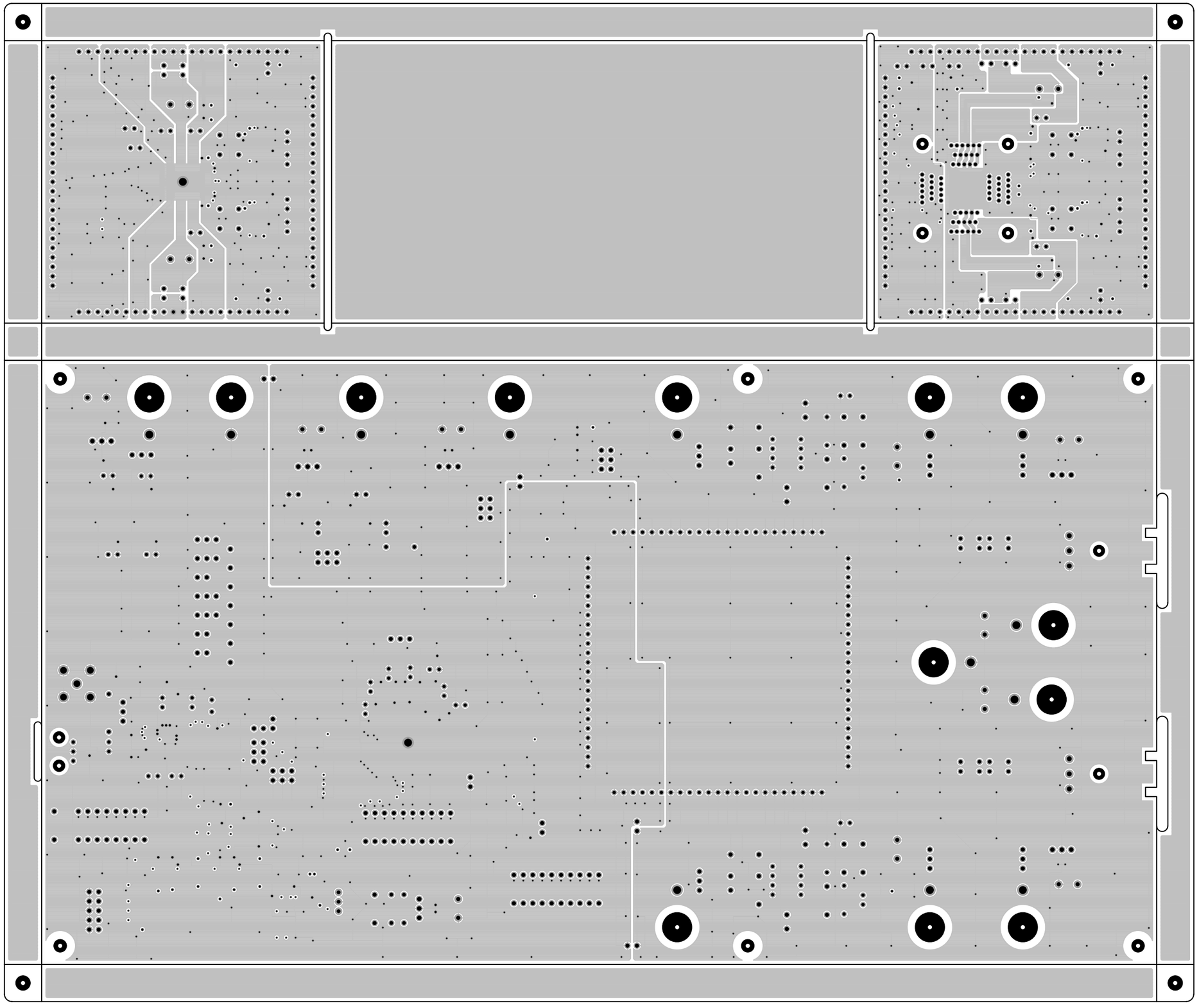
半田面シルク図　(部品面透視図)



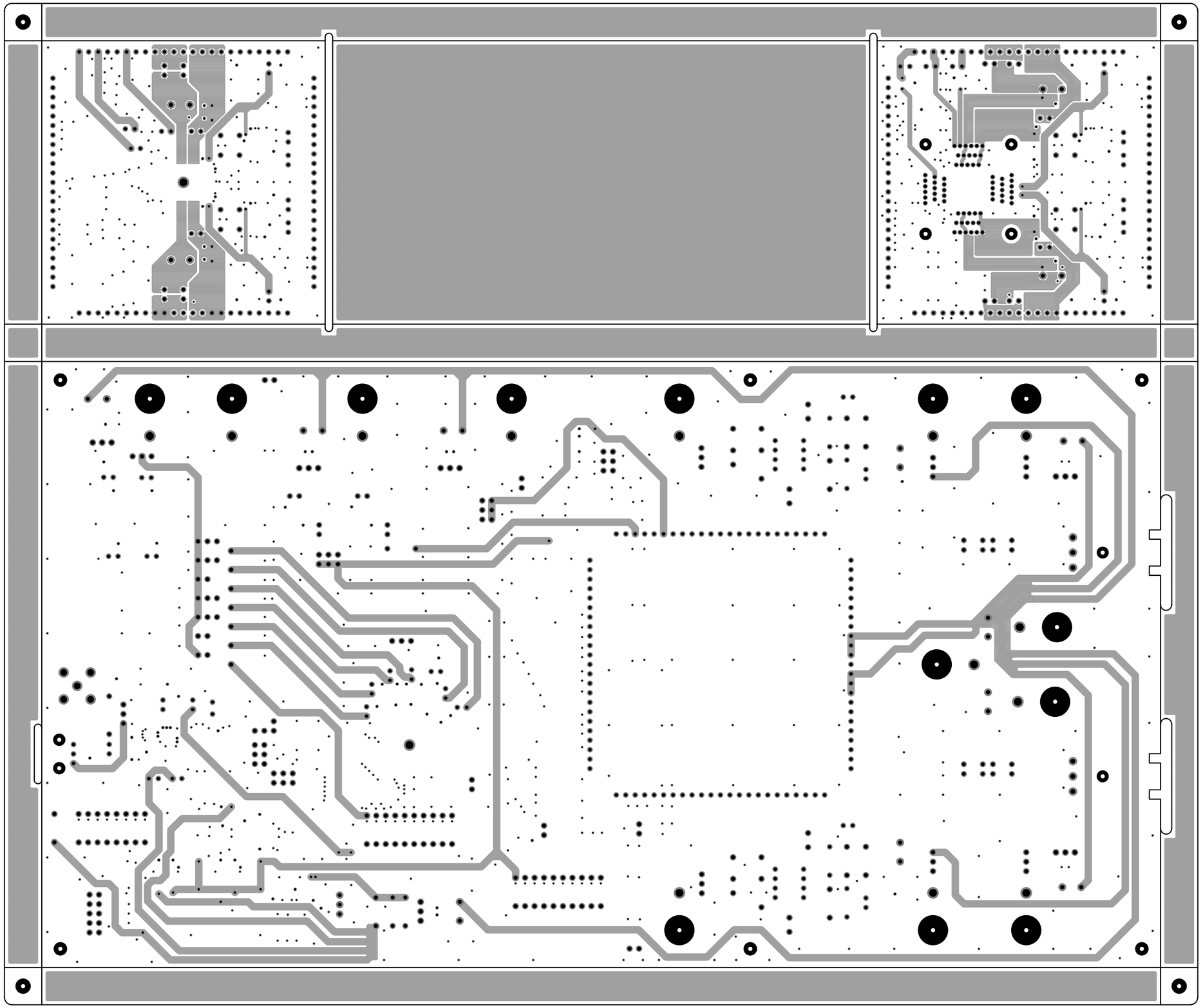
部品面パターン図（部品面透視図）



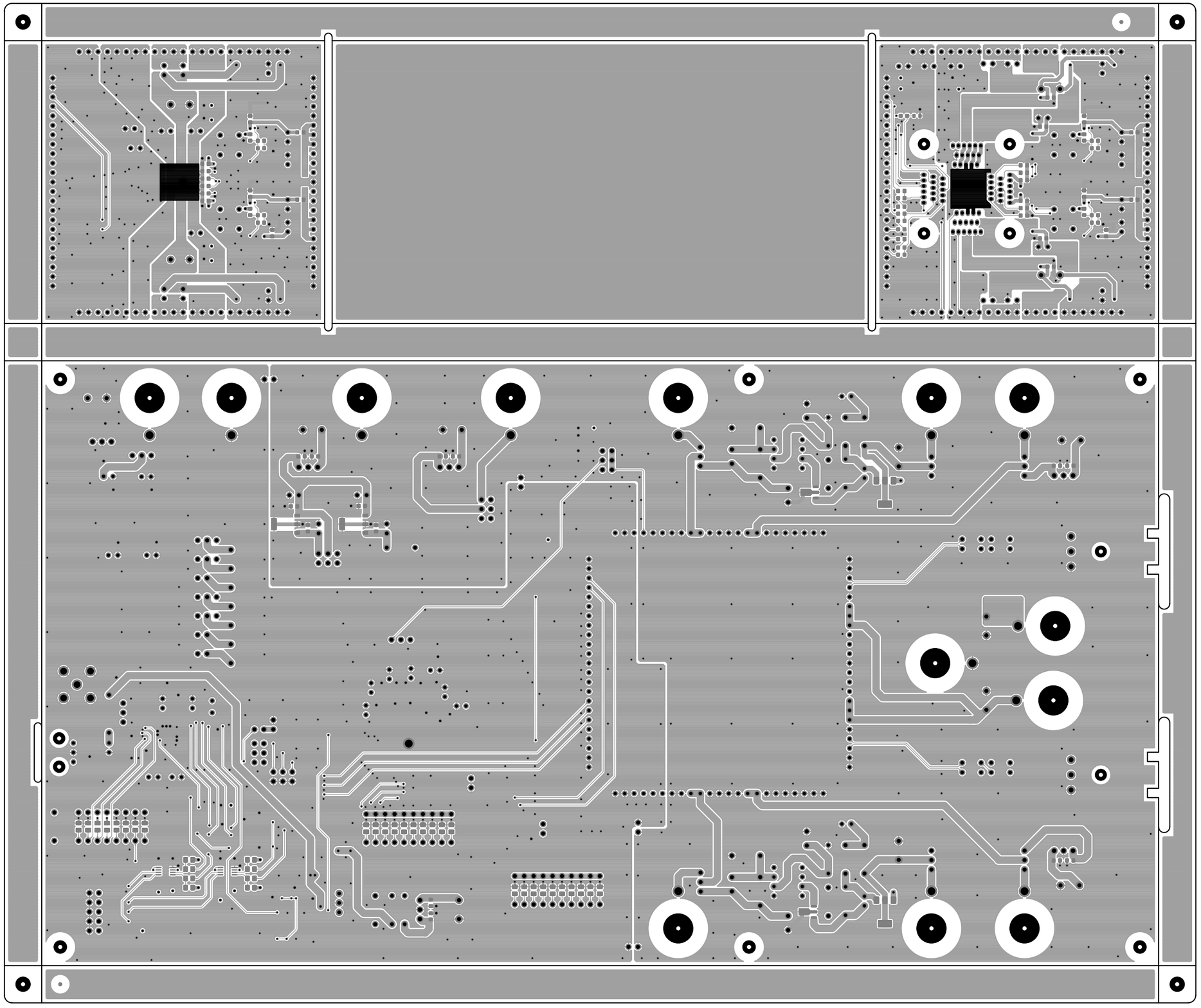
L2パターン　　(部品面透視図)



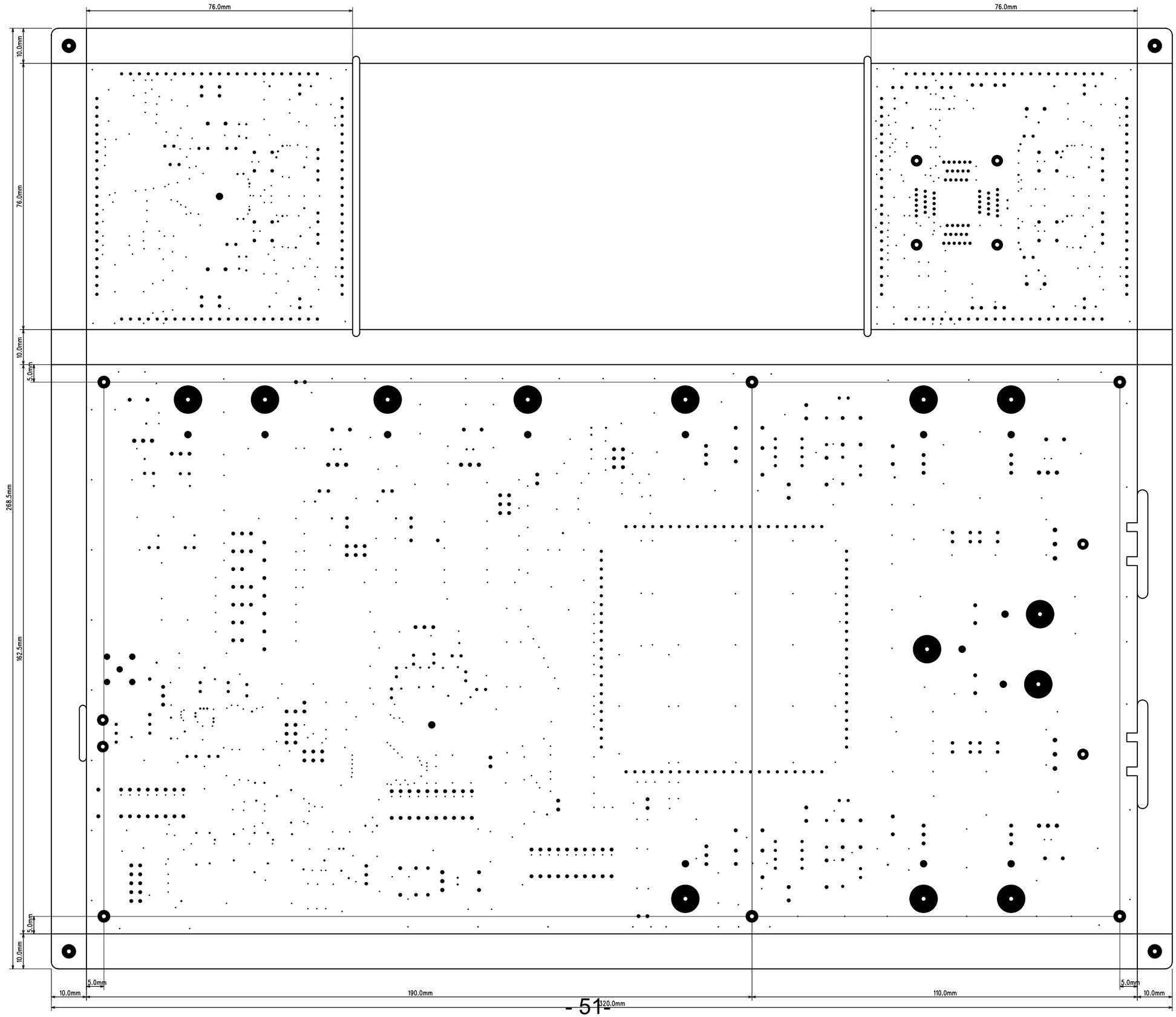
L3パターン　　(部品面透視図)



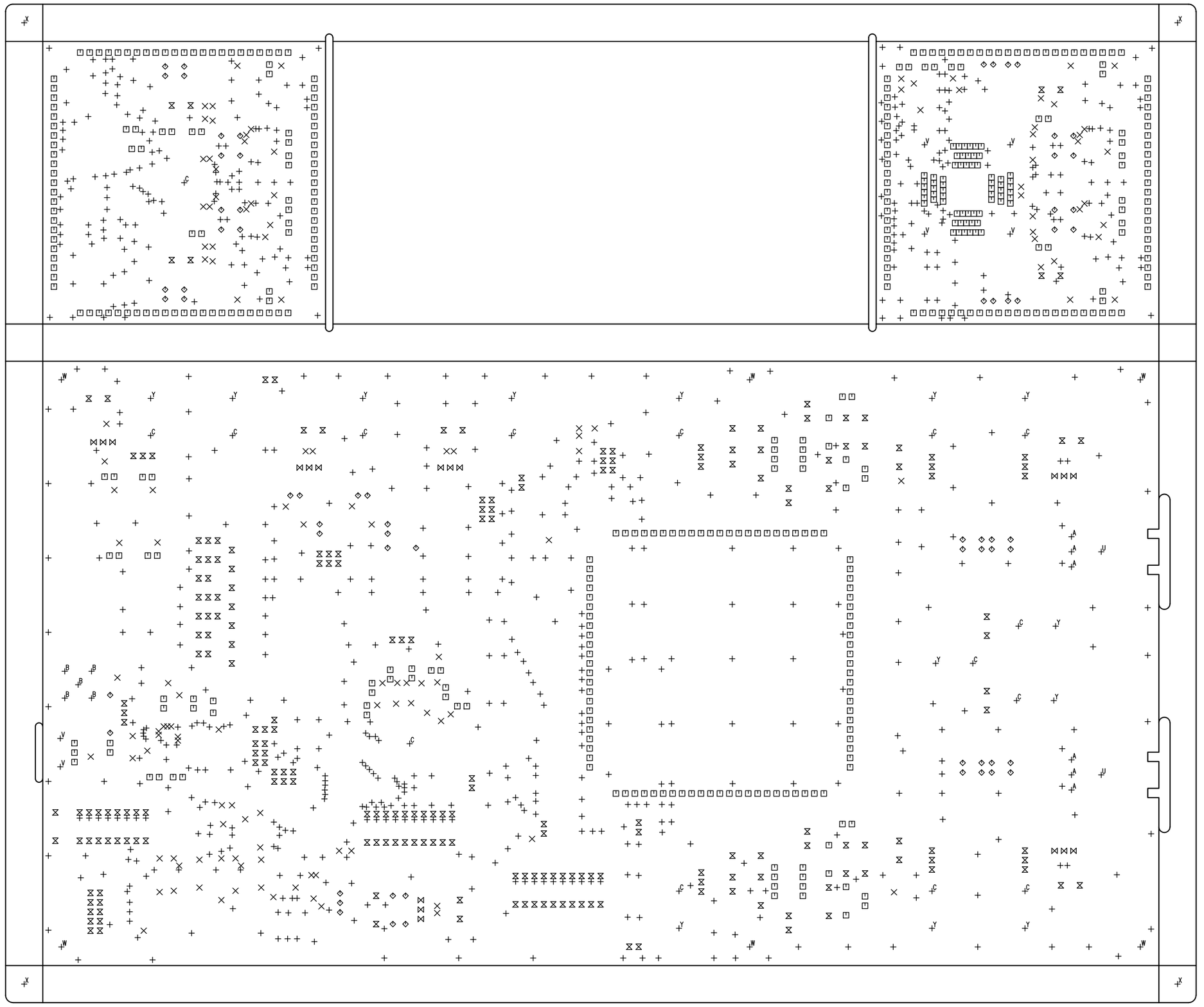
半田面パターン図（部品面透視図）



外形図、寸法図　(部品面透視図)



穴径図　　(部品面透視図)



寸法	個数	記号	PLTD
0.3	821	＋	PLTD
0.5	137	×	PLTD
0.8	453	□	PLTD
0.9	67	◇	PLTD
1	228	⧖	PLTD
1.1	18	⋈	PLTD
1.2	6	A	PLTD
1.7	5	B	PLTD
2	15	C	PLTD
3.1	2	U	NPLTD
3.2	6	V	NPLTD
3.5	6	W	NPLTD
4	4	X	NPLTD
8	13	Y	NPLTD

※　ＰＬＴＤはスルーホールです。
※　ＮＰＬＴＤはノンスルーホールです。
※　穴径は全て仕上がり径でお願いいたします。
※　指示なき穴径公差は±0.05mm

AKD4499EX-A_Rev0

(部品面透視図)